FIG.1

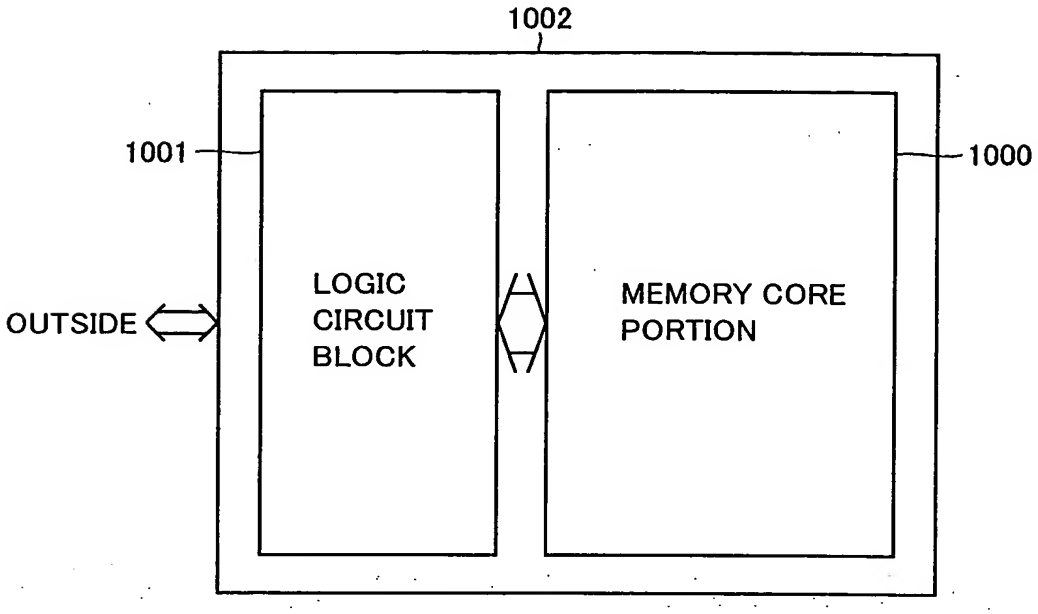

1002
1001
1000
OUTSIDE
LOGIC CIRCUIT BLOCK
MEMORY CORE PORTION

FIG.2

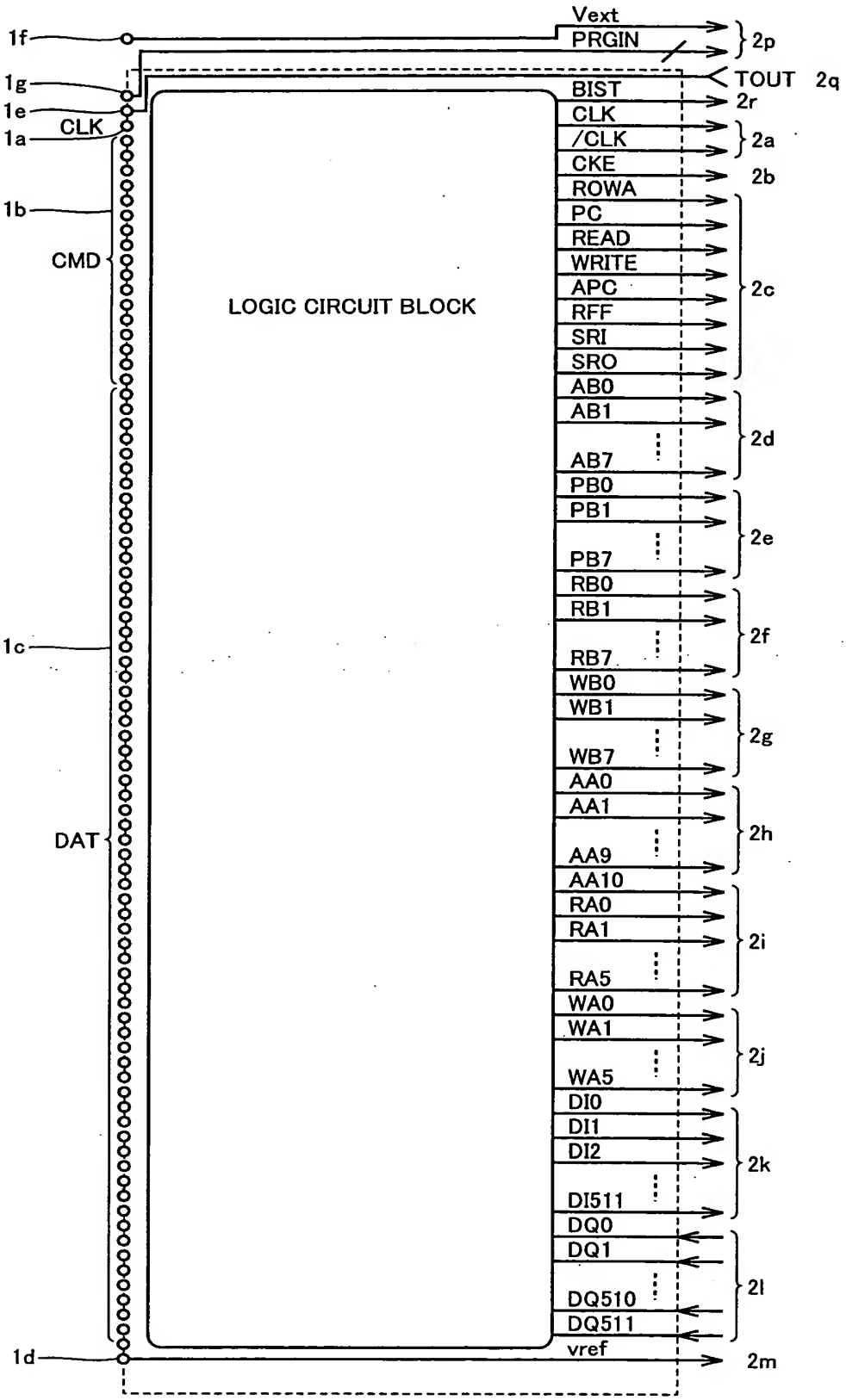
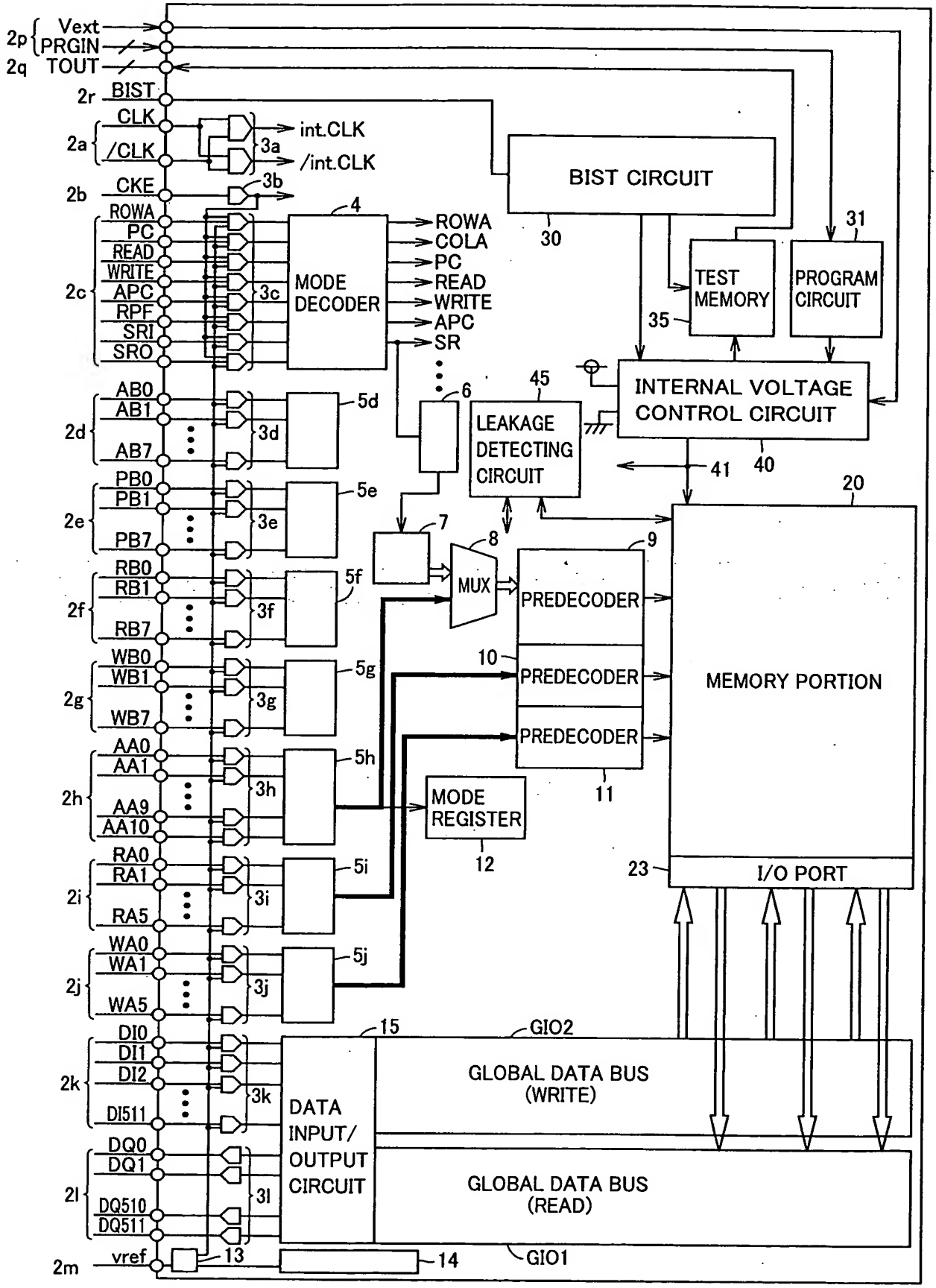

1f
1g
1e
CLK
1a
1b
CMD
1c
DAT
1d
LOGIC CIRCUIT BLOCK
Vext
PRGIN
2p
TOUT
2q
BIST
2r
CLK
/CLK
2a
CKE
2b
ROWA
PC
READ
WRITE
APC
RFF
SRI
SRO
2c
AB0
AB1
AB7
2d
PB0
PB1
PB7
2e
RB0
RB1
RB7
2f
WB0
WB1
WB7
2g
AA0
AA1
AA9
2h
AA10
RA0
RA1
RA5
2i
WA0
WA1
WA5
2j
DI0
DI1
DI2
DI511
2k
DQ0
DQ1
DQ510
DQ511
2l
vref
2m

FIG.3


2p
Vext
PRGIN
2q
TOUT
2r
BIST
2a
CLK
/CLK
3a
int.CLK
/int.CLK
2b
CKE
3b
2c
ROWA
PC
READ
WRITE
APC
RPF
SRI
SRO
3c
4
MODE DECODER
ROWA
COLA
PC
READ
WRITE
APC
SR
BIST CIRCUIT
30
31
TEST MEMORY
PROGRAM CIRCUIT
35
45
INTERNAL VOLTAGE CONTROL CIRCUIT
LEAKAGE DETECTING CIRCUIT
41
40
20
6
7
8
9
MUX
PREDECODER
PREDECODER
PREDECODER
10
11
MEMORY PORTION
2d
AB0
AB1
AB7
3d
5d
2e
PB0
PB1
PB7
3e
5e
2f
RB0
RB1
RB7
3f
5f
2g
WB0
WB1
WB7
3g
5g
2h
AA0
AA1
AA9
AA10
3h
5h
MODE REGISTER
12
23
I/O PORT
2i
RA0
RA1
RA5
3i
5i
2j
WA0
WA1
WA5
3j
5j
15
GIO2
2k
DI0
DI1
DI2
DI511
3k
DATA INPUT/ OUTPUT CIRCUIT
GLOBAL DATA BUS (WRITE)
GLOBAL DATA BUS (READ)
2l
DQ0
DQ1
DQ510
DQ511
3l
2m
vref
13
14
GIO1

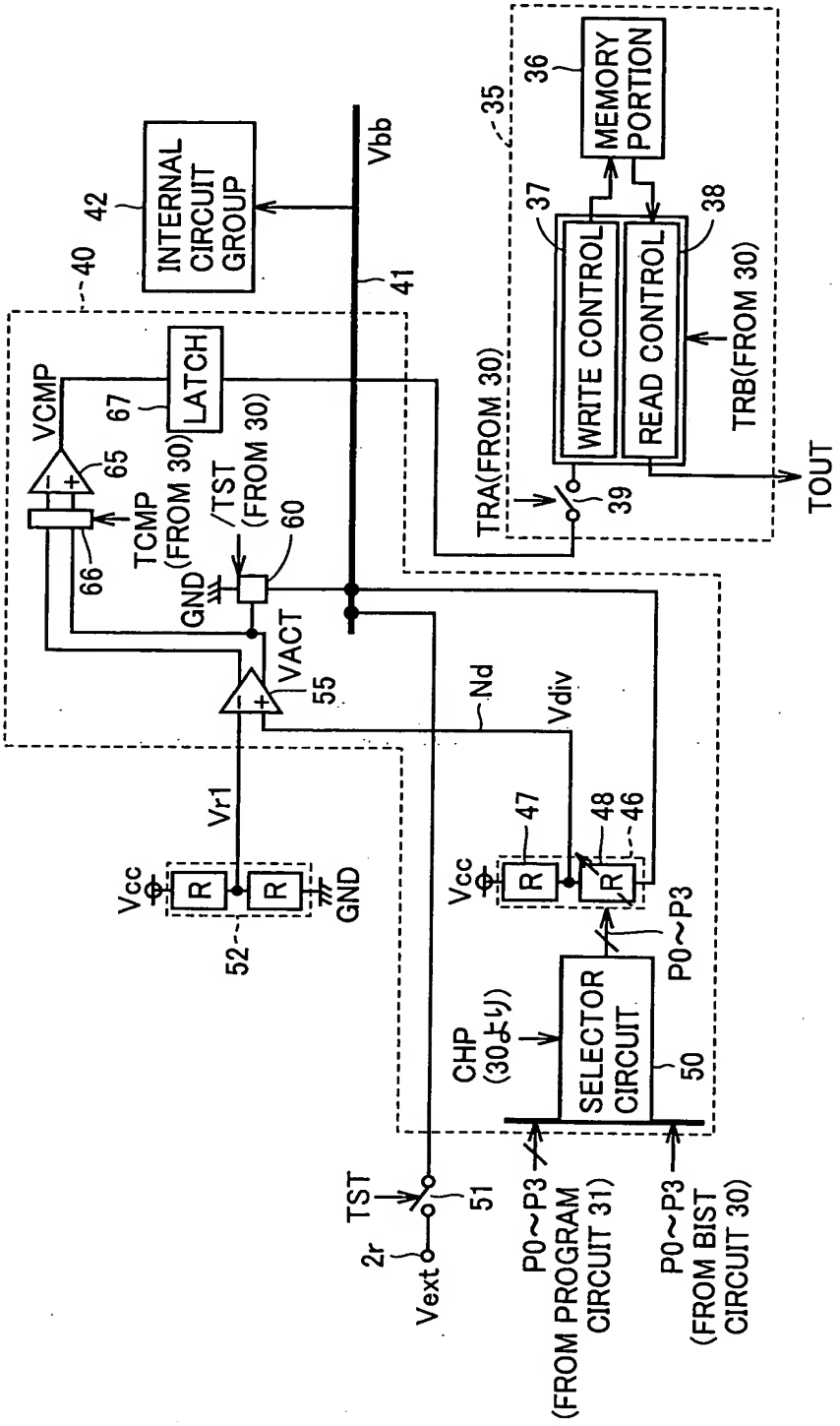

INTERNAL CIRCUIT GROUP
42
40
Vbb
41
35
36
MEMORY PORTION
37
38
WRITE CONTROL
READ CONTROL
TRB(FROM 30)
TOUT
TRA(FROM 30)
39
LATCH
67
VCMP
65
66
TCMP (FROM 30)
/TST (FROM 30)
60
GND
VACT
55
Nd
Vdiv
Vr1
Vcc
R
R
GND
52
47
48
46
P0~P3
CHP (30より)
SELECTOR CIRCUIT
50
TST
51
2r
Vext
P0~P3 (FROM PROGRAM CIRCUIT 31)
P0~P3 (FROM BIST CIRCUIT 30)

FIG.4

FIG.5

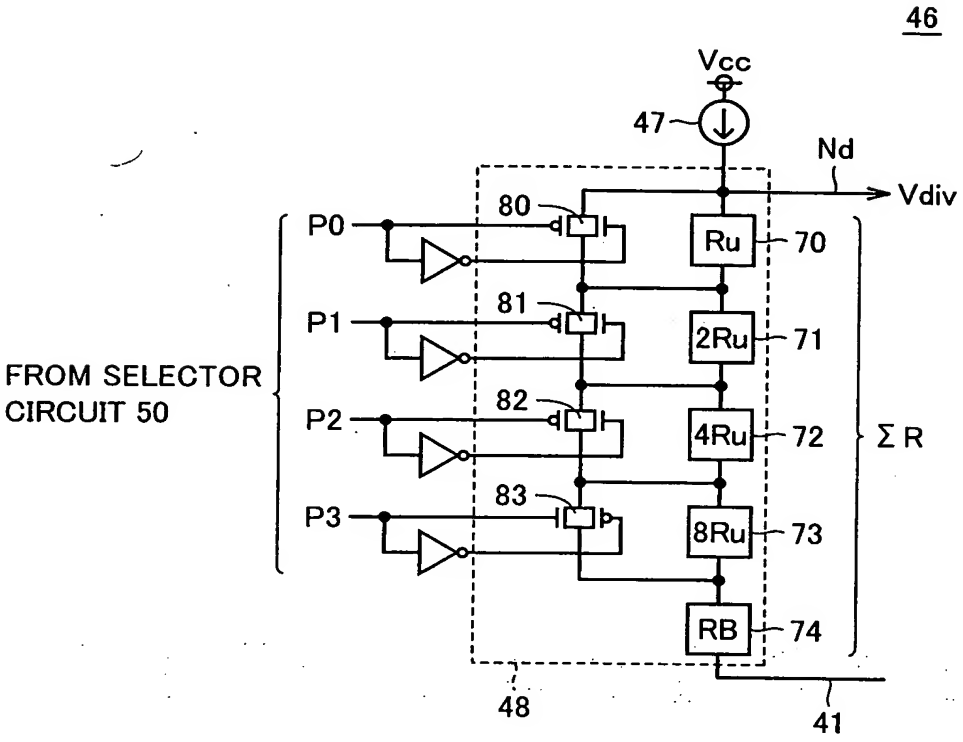

46
Vcc
47
Nd
Vdiv
80
81
82
83
P0
P1
P2
P3
FROM SELECTOR CIRCUIT 50
Ru
2Ru
4Ru
8Ru
RB
70
71
72
73
74
Σ R
48
41

FIG.6

LOW Vbb ⟵⟶ HIGH Vbb

ADJUSTMENT LEVEL		−8	−7	−6	−5	−4	−3	−2	−1	0	+1	+2	+3	+4	+5	+6	+7
ADJUSTMENT SIGNALS (FROM BIST CIRCUIT 30)	P0	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
	P1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
	P2	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
	P3	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
VCMP LEVEL		H	H	H	H	H	H	L	L	L	L	L	L	L	L	L	L
OUTPUT OF EX-OR 93		L	L	L	L	L	L	H	L	L	L	L	L	L	L	L	L

ADJUSTMENT SIGNALS ACCUMULATED TO MEMORY 36

- P0=1
- P1=0
- P2=1
- P3=1

FIG.7

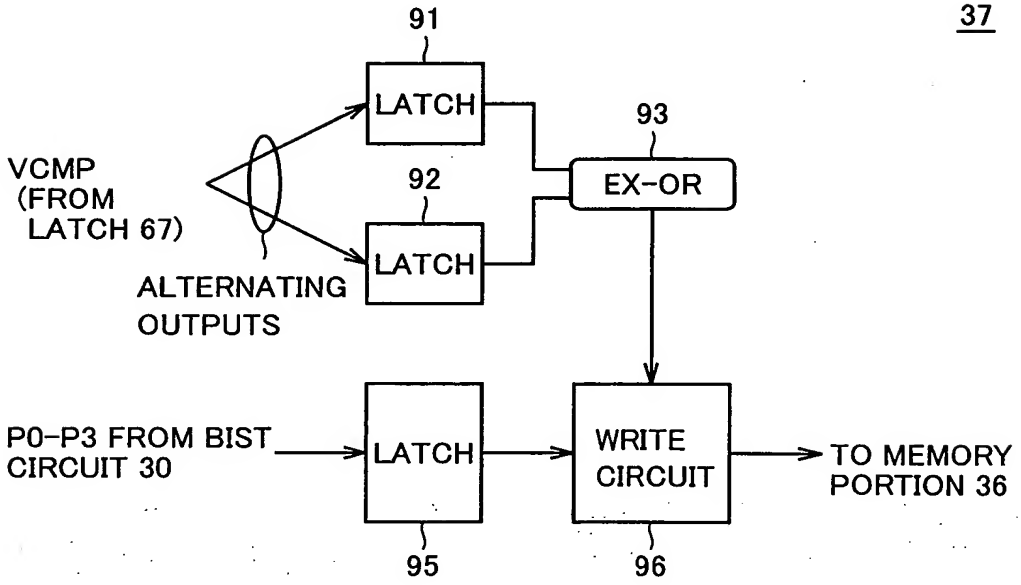

37
91
LATCH
93
VCMP
(FROM
LATCH 67)
92
EX-OR
LATCH
ALTERNATING
OUTPUTS
P0-P3 FROM BIST
CIRCUIT 30
LATCH
WRITE
CIRCUIT
TO MEMORY
PORTION 36
95
96

FIG.8

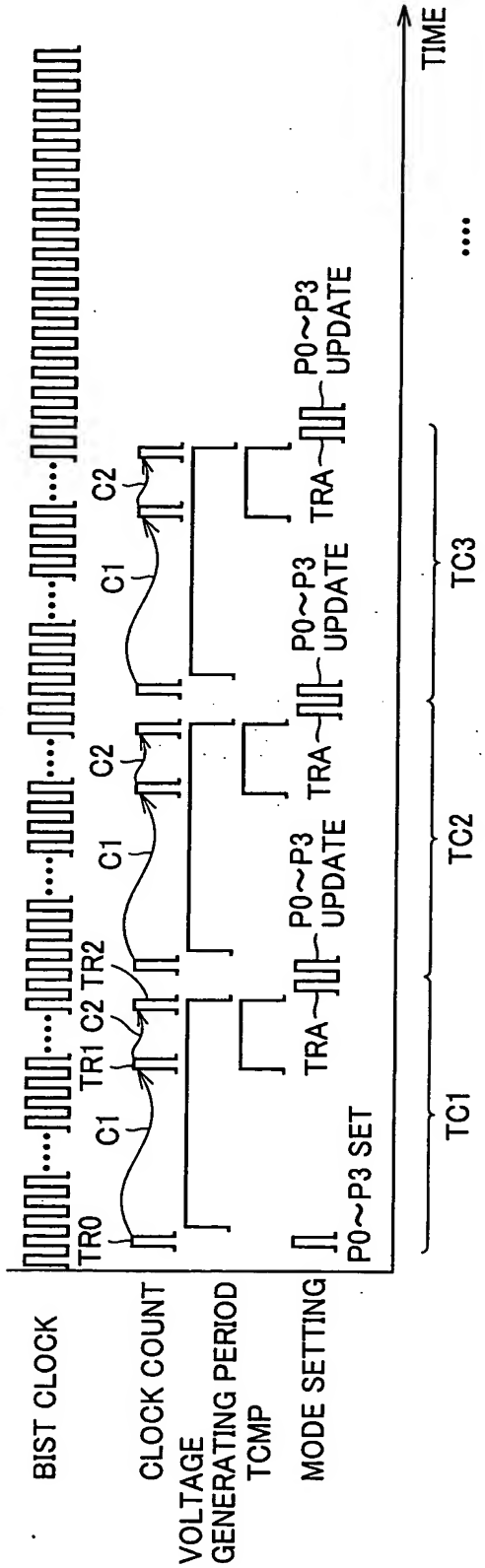
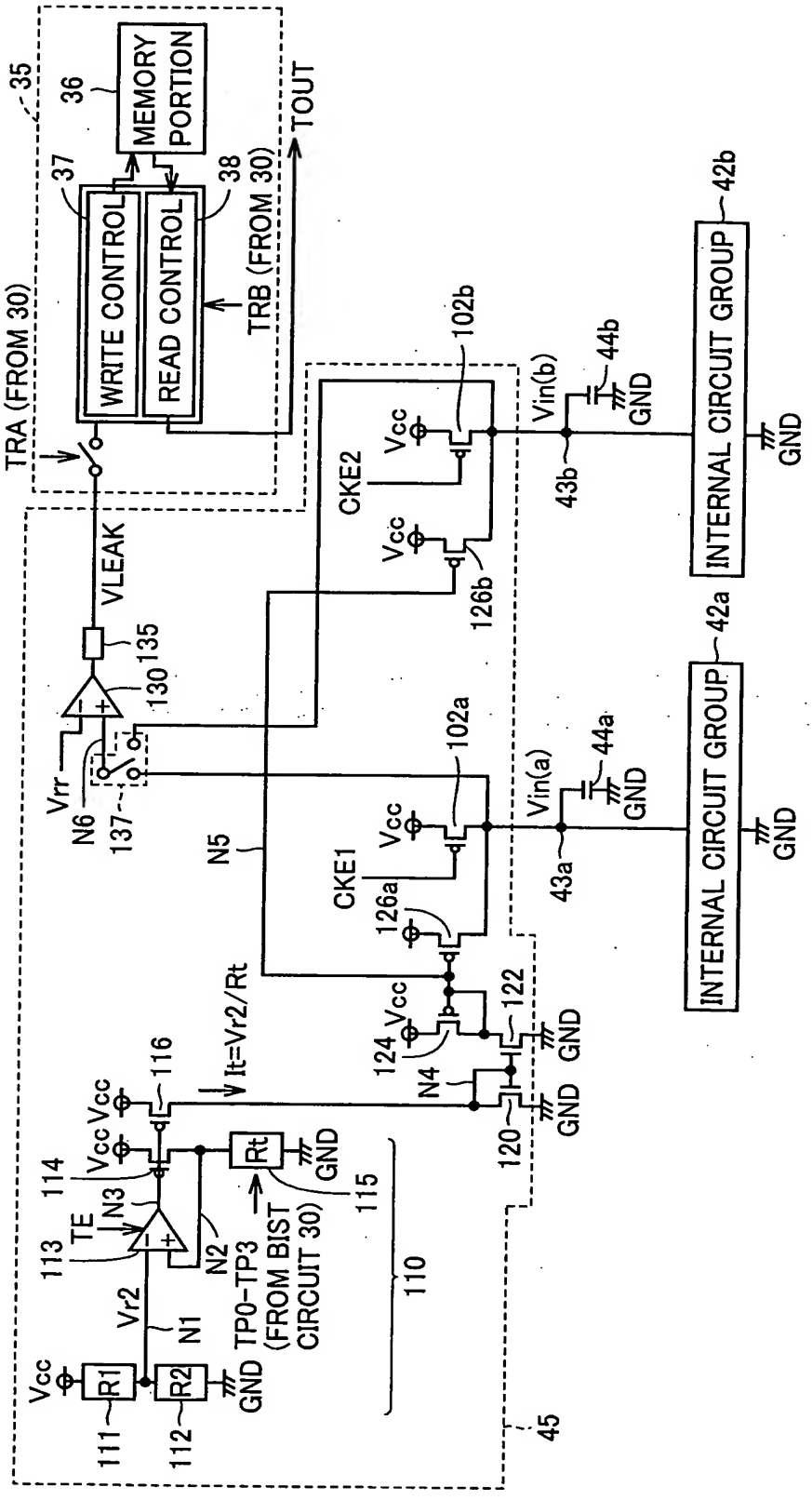

BIST CLOCK
CLOCK COUNT
VOLTAGE GENERATING PERIOD TCMP
MODE SETTING
TIME
TR0
C1
TR1
C2
TR2
C1
C2
C1
C2
P0~P3 SET
TRA
P0~P3 UPDATE
TRA
P0~P3 UPDATE
TRA
P0~P3 UPDATE
TC1
TC2
TC3
....

FIG.9


35
36
MEMORY PORTION
37
WRITE CONTROL
READ CONTROL
38
TRB (FROM 30)
TOUT
TRA (FROM 30)
VLEAK
135
130
Vrr
N6
137
N5
CKE2
CKE1
Vcc
102b
102a
126b
126a
124
122
120
116
It=Vr2/Rt
N4
Vin(b)
Vin(a)
44b
44a
GND
43b
43a
42b
42a
INTERNAL CIRCUIT GROUP
114
N3
113
TE
Vr2
N1
N2
TP0-TP3
(FROM BIST CIRCUIT 30)
Rt
115
110
R1
R2
111
112
45

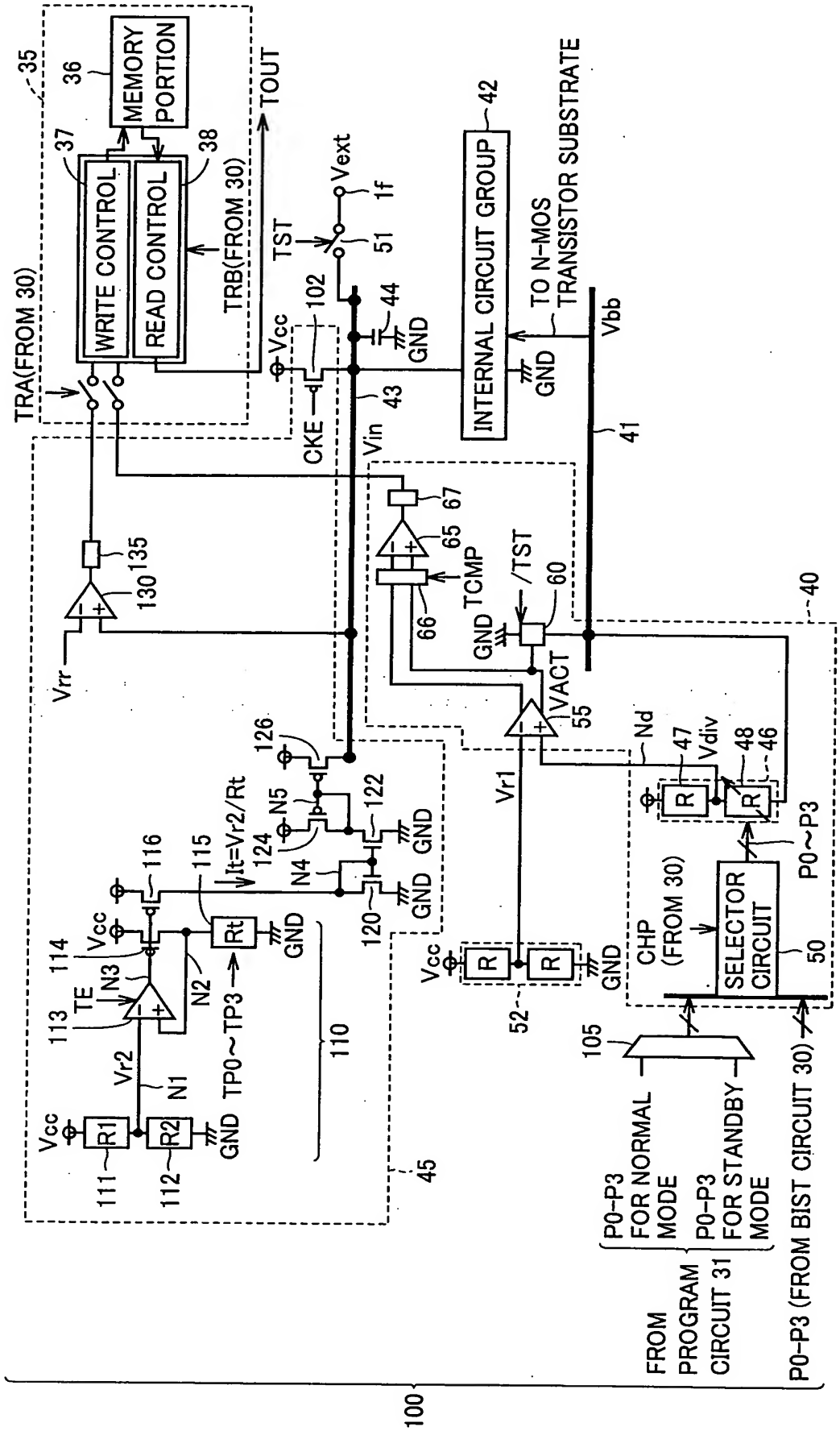

MEMORY PORTION
WRITE CONTROL
READ CONTROL
TRA(FROM 30)
TRB(FROM 30)
TOUT
TST
Vext
INTERNAL CIRCUIT GROUP
TO N-MOS TRANSISTOR SUBSTRATE
Vbb
GND
Vcc
CKE
Vin
Vrr
TCMP
/TST
VACT
Nd
Vdiv
Vr1
Vr2
It=Vr2/Rt
TE
TP0~TP3
CHP (FROM 30)
SELECTOR CIRCUIT
P0~P3
P0-P3 FOR NORMAL MODE
P0-P3 FOR STANDBY MODE
FROM PROGRAM CIRCUIT 31
P0-P3 (FROM BIST CIRCUIT 30)

FIG.10

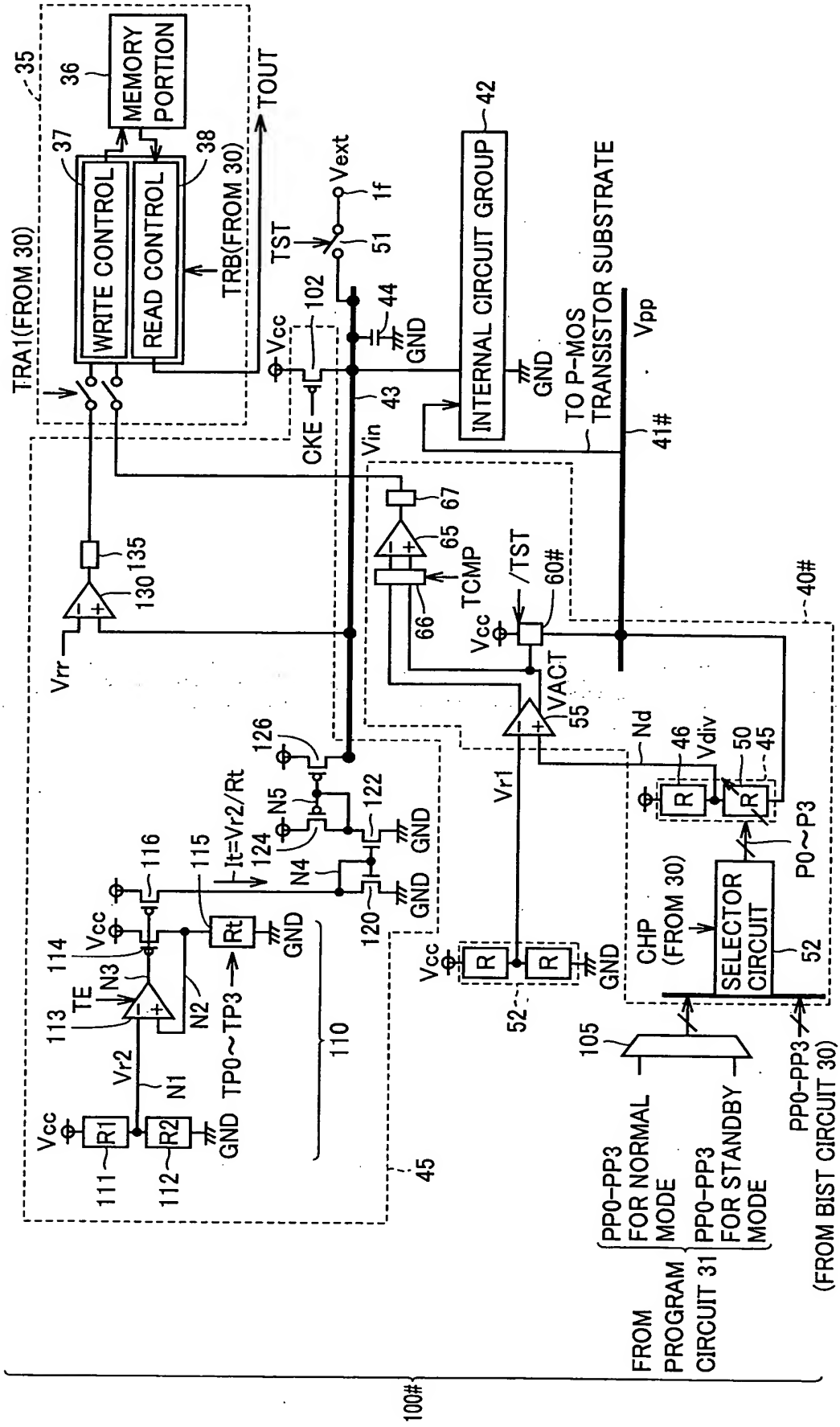

35
36
MEMORY PORTION
37
WRITE CONTROL
READ CONTROL
38
TRA1(FROM 30)
TRB(FROM 30)
TOUT
TST
Vext
1f
51
102
44
GND
Vcc
CKE
43
Vin
INTERNAL CIRCUIT GROUP
42
GND
TO P-MOS TRANSISTOR SUBSTRATE
Vpp
41#
67
65
TCMP
66
/TST
60#
Vcc
VACT
55
40#
Vrr
130
135
126
N5
122
GND
124
It=Vr2/Rt
N4
116
115
120
Vcc
114
N3
TE
113
N2
Rt
GND
Vr2
N1
TP0~TP3
110
Vcc
R1
R2
GND
111
112
45
Vr1
Nd
46
Vdiv
50
45
R
52
Vcc
GND
CHP (FROM 30)
SELECTOR CIRCUIT
P0~P3
105
PP0-PP3 FOR NORMAL MODE
PP0-PP3 FOR STANDBY MODE
FROM PROGRAM CIRCUIT 31
PP0-PP3 (FROM BIST CIRCUIT 30)
100#

FIG.11

FIG.12

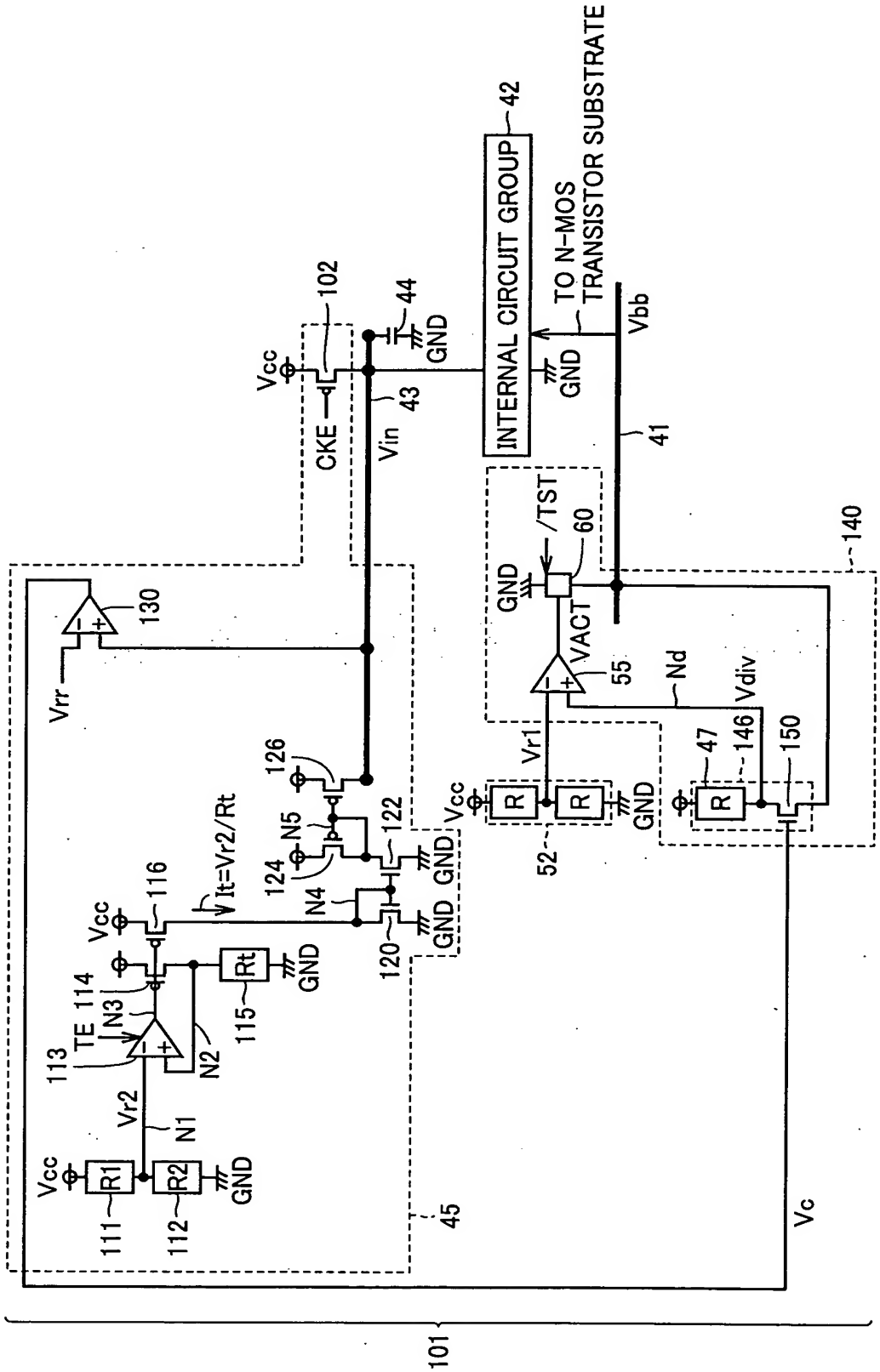

INTERNAL CIRCUIT GROUP
42
TO N-MOS TRANSISTOR SUBSTRATE
Vbb
41
Vcc
102
44
GND
CKE
Vin
43
/TST
60
140
130
Vrr
VACT
55
Nd
Vdiv
Vr1
47
146
150
126
N5
122
124
N4
120
116
It=Vr2/Rt
Rt
115
TE
114
N3
113
N2
Vr2
N1
R1
R2
111
112
R
52
45
Vc
101

FIG.13

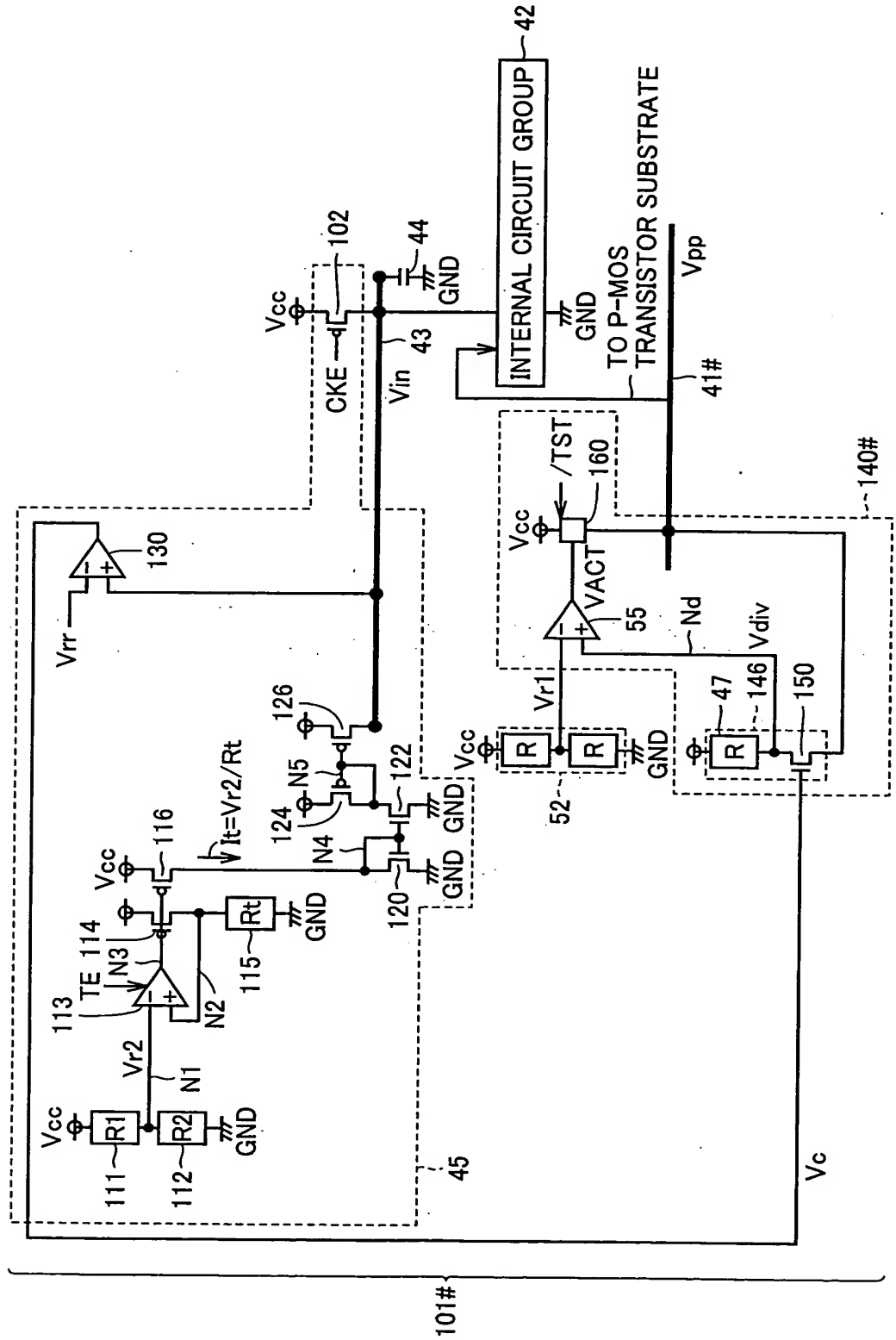

INTERNAL CIRCUIT GROUP
42
TO P-MOS TRANSISTOR SUBSTRATE
Vpp
41#
Vcc
102
CKE
44
GND
43
Vin
/TST
160
140#
VACT
55
Nd
Vdiv
Vr1
47
146
150
R
52
130
Vrr
126
N5
122
124
N4
120
116
It=Vr2/Rt
Rt
115
TE
114
N3
N2
113
Vr2
N1
R1
R2
111
112
45
Vc
101#

FIG.14

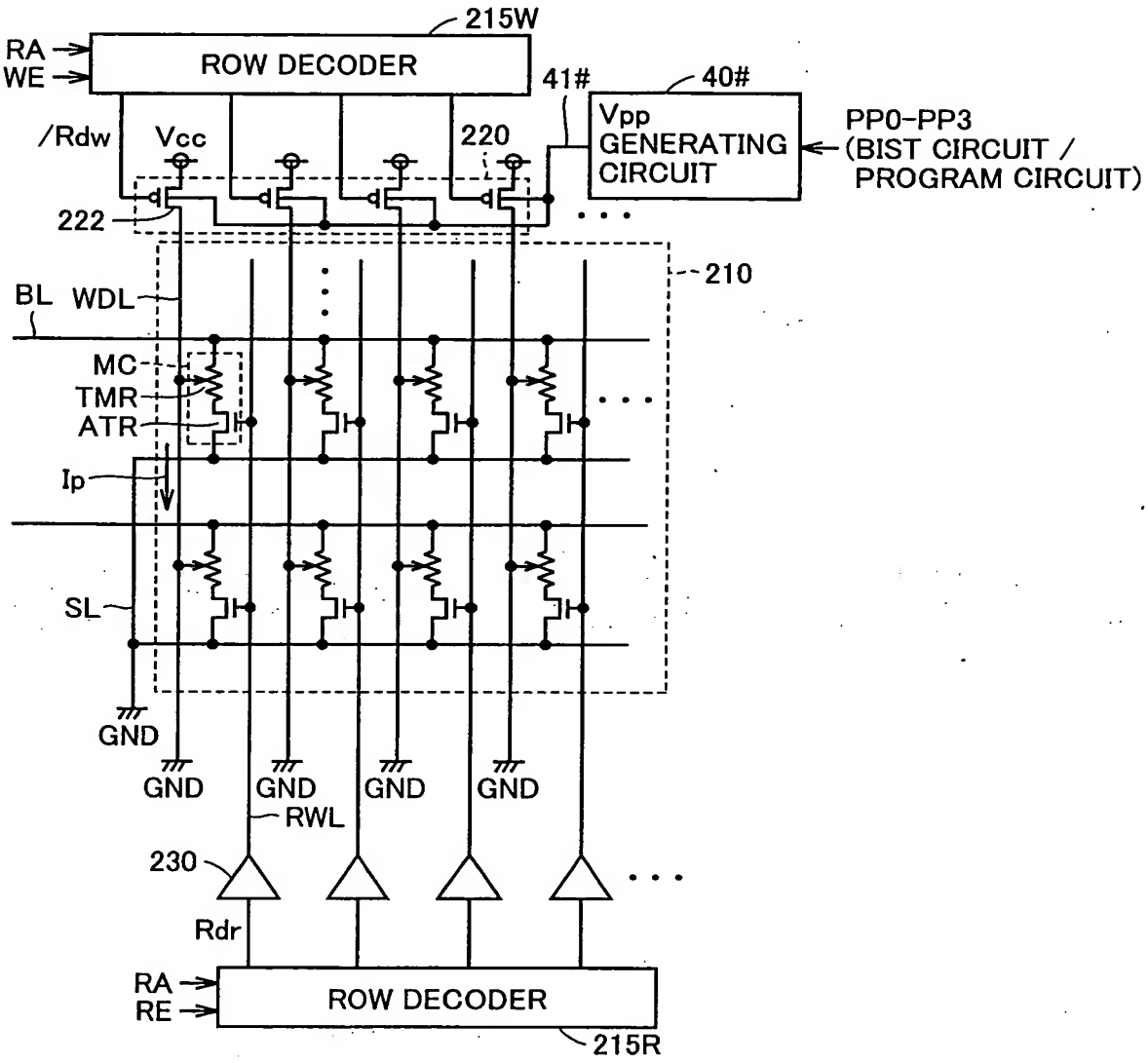

215W
RA
WE
ROW DECODER
41#
40#
Vpp GENERATING CIRCUIT
PP0-PP3 (BIST CIRCUIT / PROGRAM CIRCUIT)
/Rdw
Vcc
220
222
210
BL
WDL
MC
TMR
ATR
Ip
SL
GND
RWL
230
Rdr
RA
RE
ROW DECODER
215R

FIG.15

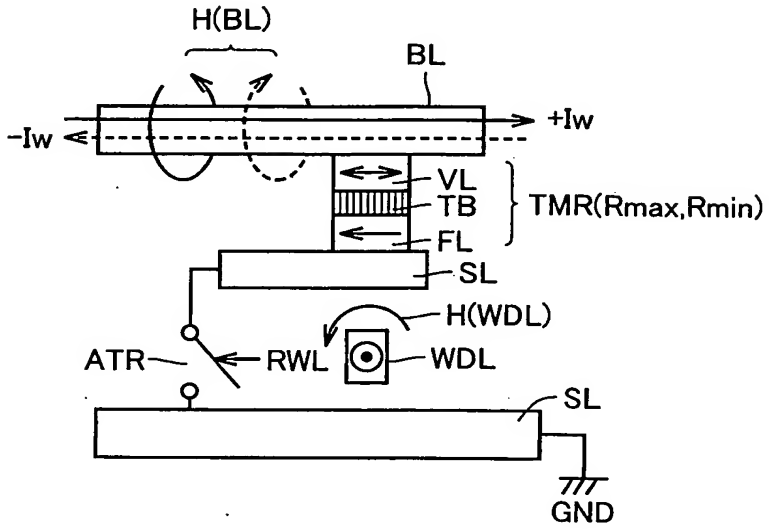

H(BL)
BL
-Iw
+Iw
VL
TB
FL
TMR(Rmax,Rmin)
SL
H(WDL)
ATR
RWL
WDL
SL
GND

FIG.16

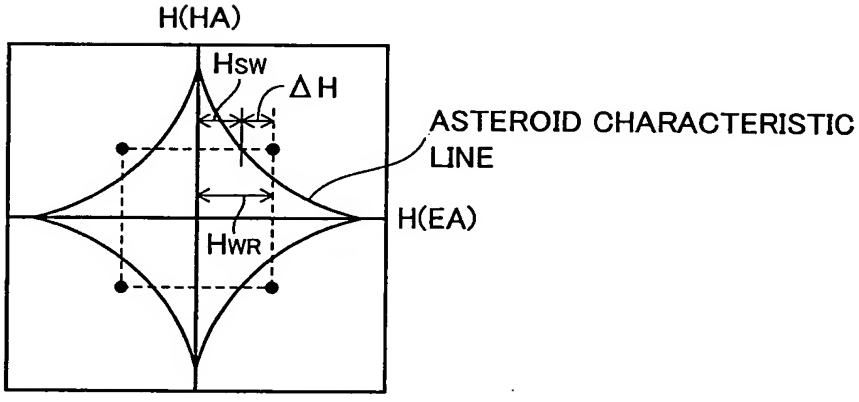
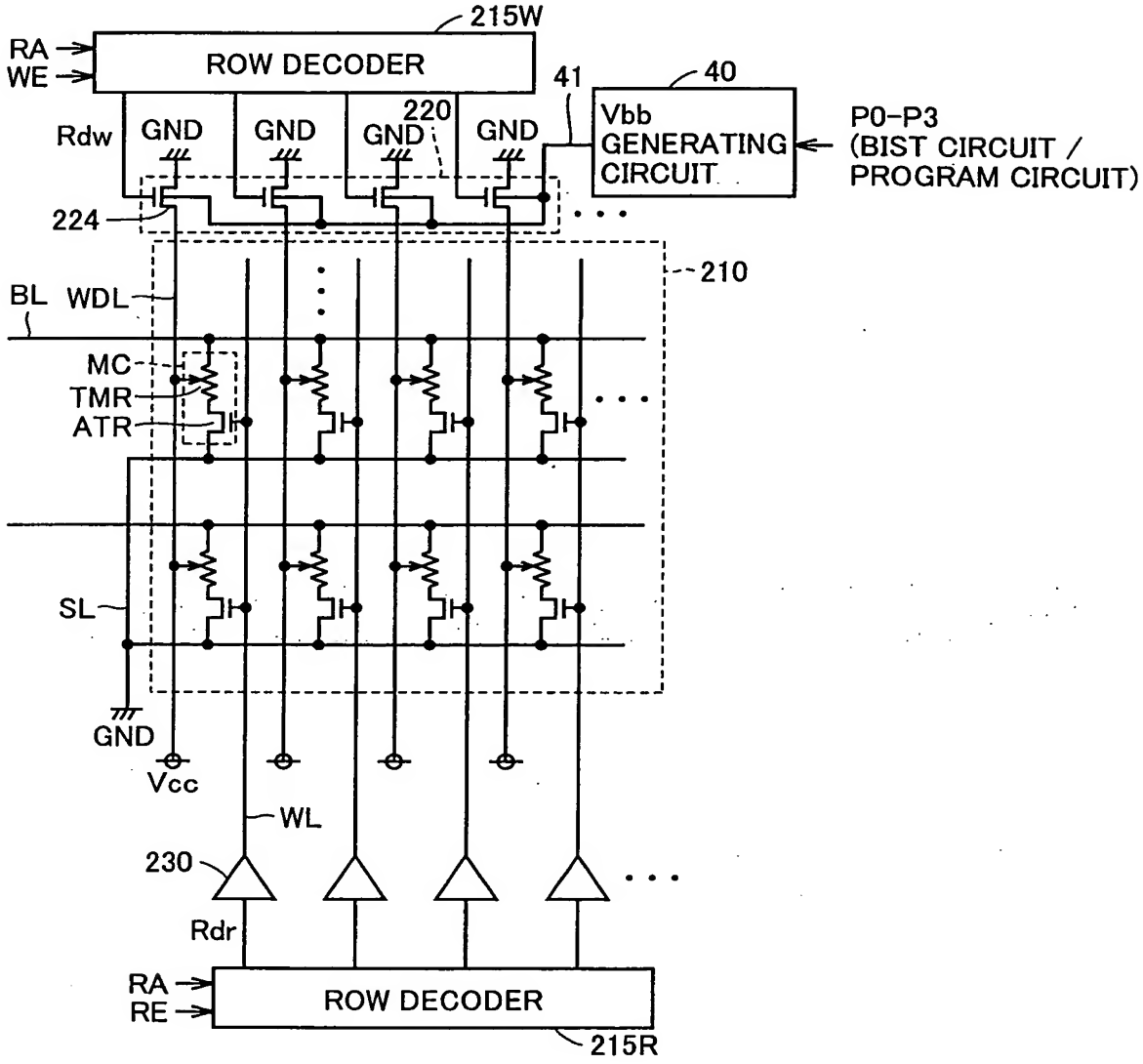

H(HA)
Hsw
ΔH
ASTEROID CHARACTERISTIC LINE
H(EA)
Hwr

FIG.17


215W
RA
WE
ROW DECODER
41
40
220
Rdw
GND
GND
GND
GND
Vbb
GENERATING
CIRCUIT
P0-P3
(BIST CIRCUIT /
PROGRAM CIRCUIT)
224
210
BL
WDL
MC
TMR
ATR
SL
GND
Vcc
WL
230
Rdr
RA
RE
ROW DECODER
215R

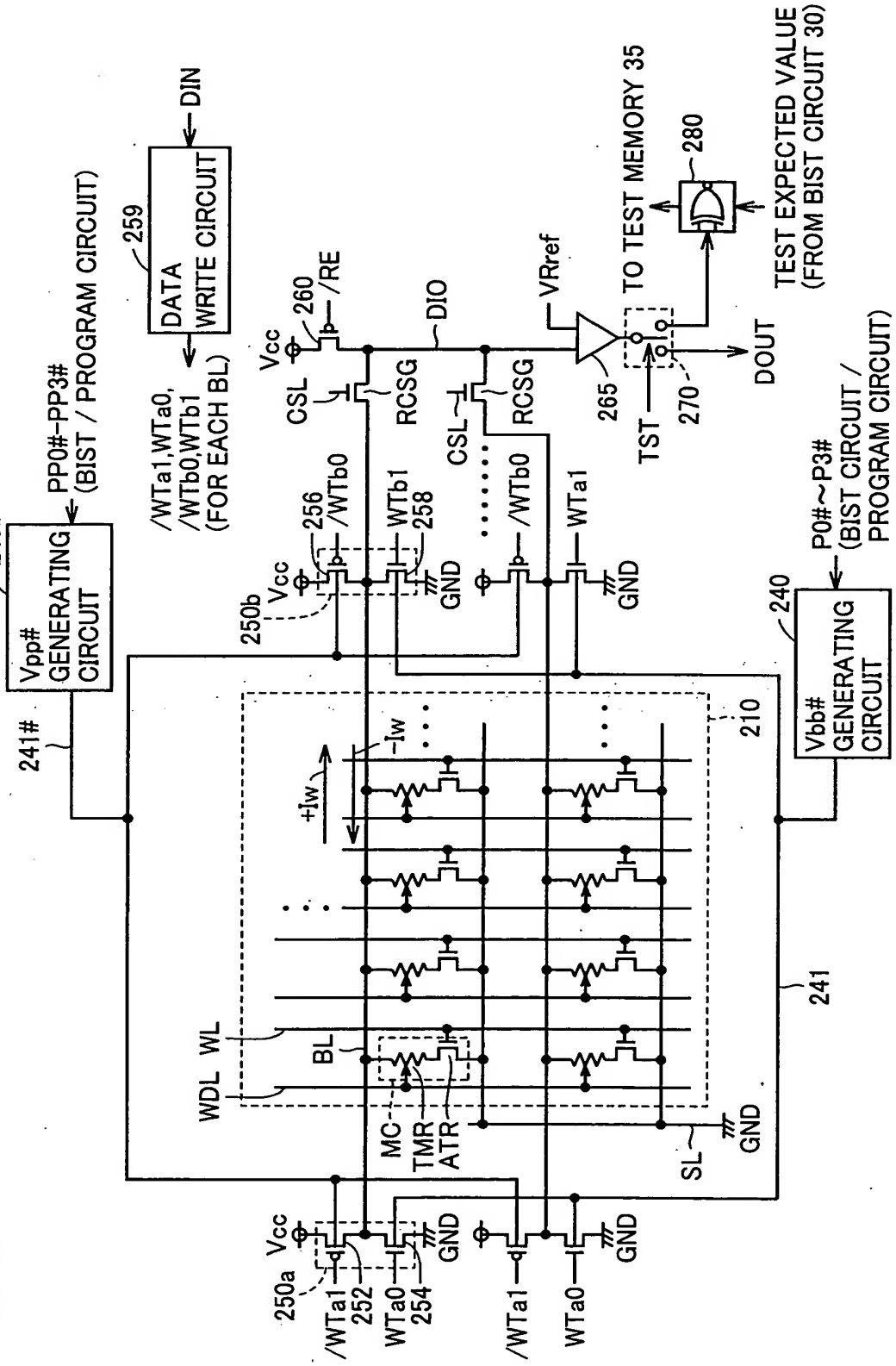

DIN
259
DATA WRITE CIRCUIT
/WTa1,WTa0,
/WTb0,WTb1
(FOR EACH BL)
PP0#-PP3#
(BIST / PROGRAM CIRCUIT)
240#
Vpp# GENERATING CIRCUIT
241#
Vcc
260
/RE
DIO
VRref
TO TEST MEMORY 35
280
TEST EXPECTED VALUE
(FROM BIST CIRCUIT 30)
CSL
RCSG
265
TST
270
DOUT
256
/WTb0
WTb1
258
WTa1
250b
GND
240
P0#~P3#
(BIST CIRCUIT / PROGRAM CIRCUIT)
Vbb# GENERATING CIRCUIT
210
-Iw
+Iw
WDL
WL
BL
MC
TMR
ATR
SL
241
250a
252
254

FIG.18

FIG.19

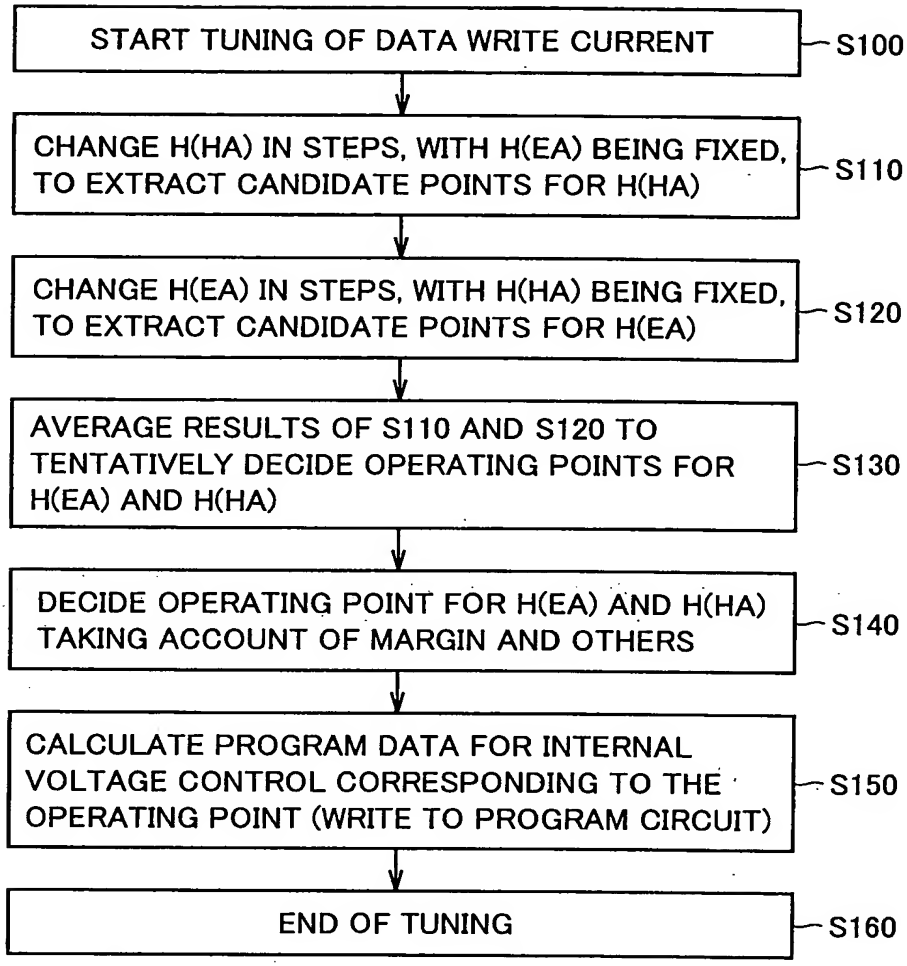

START TUNING OF DATA WRITE CURRENT
S100
CHANGE H(HA) IN STEPS, WITH H(EA) BEING FIXED, TO EXTRACT CANDIDATE POINTS FOR H(HA)
S110
CHANGE H(EA) IN STEPS, WITH H(HA) BEING FIXED, TO EXTRACT CANDIDATE POINTS FOR H(EA)
S120
AVERAGE RESULTS OF S110 AND S120 TO TENTATIVELY DECIDE OPERATING POINTS FOR H(EA) AND H(HA)
S130
DECIDE OPERATING POINT FOR H(EA) AND H(HA) TAKING ACCOUNT OF MARGIN AND OTHERS
S140
CALCULATE PROGRAM DATA FOR INTERNAL VOLTAGE CONTROL CORRESPONDING TO THE OPERATING POINT (WRITE TO PROGRAM CIRCUIT)
S150
END OF TUNING
S160

FIG.20

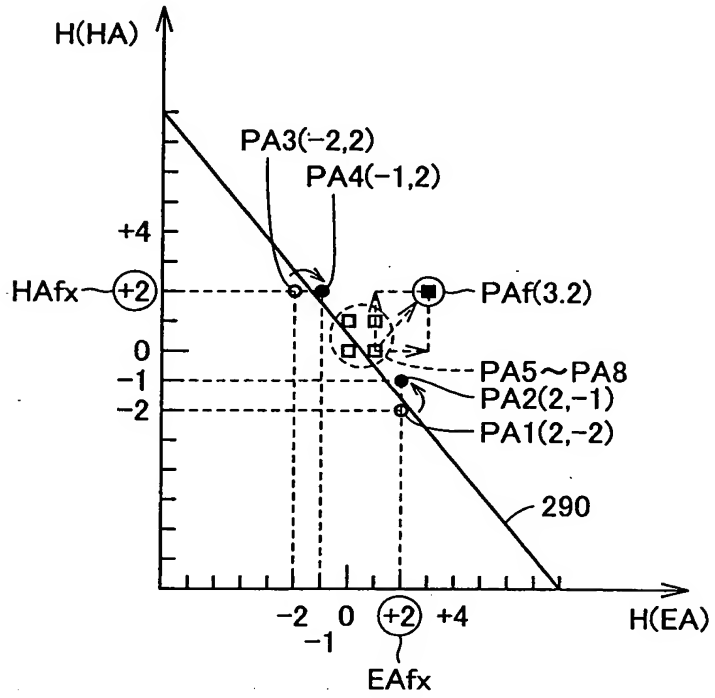

H(HA)
PA3(−2,2)
PA4(−1,2)
+4
HAfx
+2
PAf(3.2)
0
−1
−2
PA5～PA8
PA2(2,−1)
PA1(2,−2)
290
−2
−1
0
+2
+4
H(EA)
EAfx

FIG.21

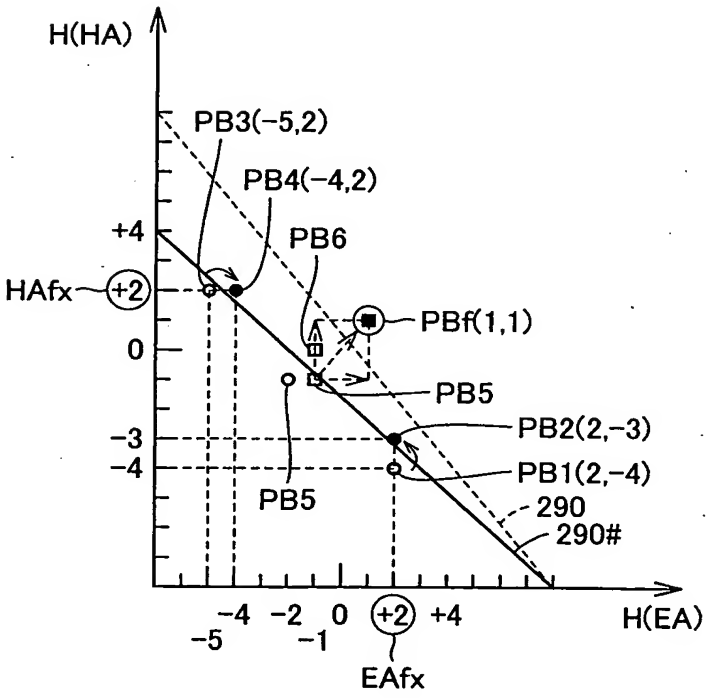

H(HA)
PB3(−5,2)
PB4(−4,2)
+4
PB6
HAfx
+2
PBf(1,1)
0
PB5
−3
PB2(2,−3)
−4
PB1(2,−4)
PB5
290
290#
−4
−5
−2
−1
0
+2
+4
H(EA)
EAfx

FIG.22

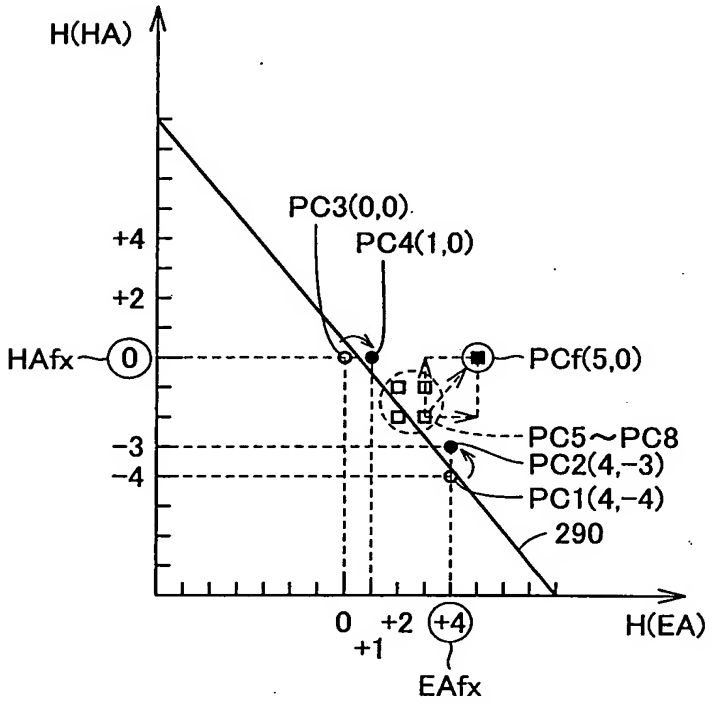
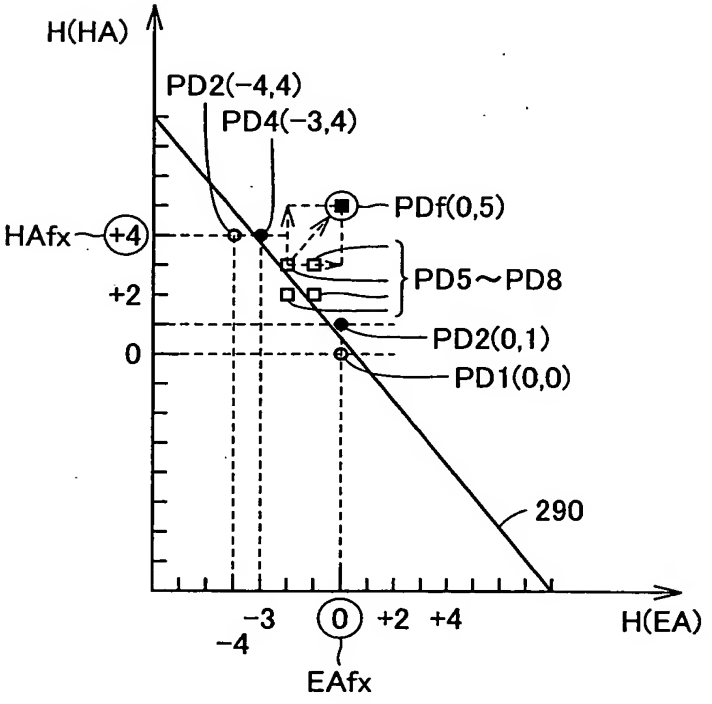

H(HA)
PC3(0,0)
PC4(1,0)
+4
+2
HAfx
0
PCf(5,0)
PC5～PC8
-3
PC2(4,-3)
-4
PC1(4,-4)
290
0
+2
+4
+1
H(EA)
EAfx

FIG.23


H(HA)
PD2(-4,4)
PD4(-3,4)
PDf(0,5)
HAfx
+4
PD5～PD8
+2
PD2(0,1)
0
PD1(0,0)
290
-3
0
+2
+4
-4
H(EA)
EAfx

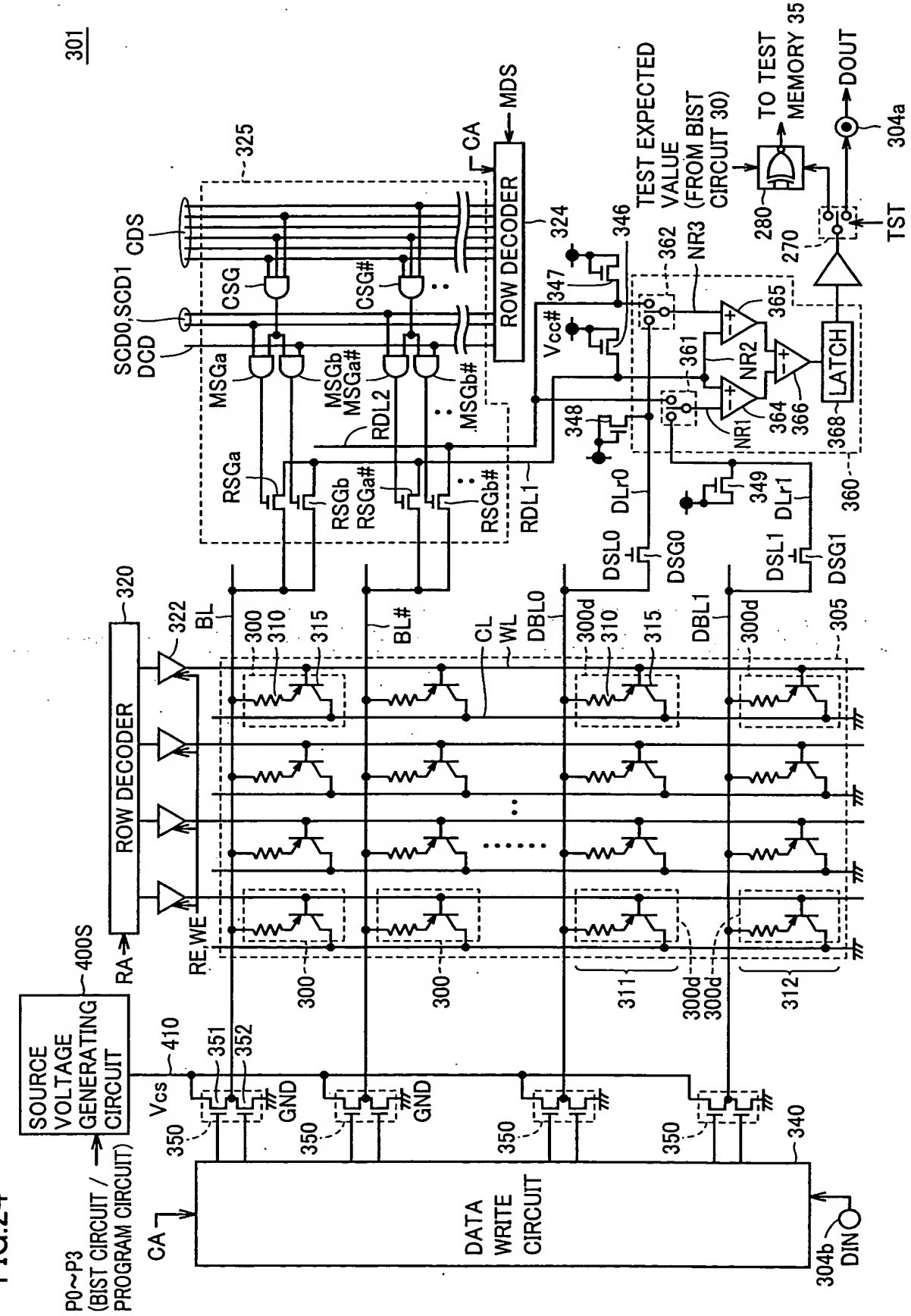

301
325
CDS
SCD0,SCD1
DCD
CSG
CSG#
MSGa
MSGb
MSGa#
MSGb#
RDL2
RSGa
RSGb
RSGa#
RSGb#
RDL1
CA
MDS
ROW DECODER
324
346
347
Vcc#
348
349
DLr0
DLr1
DSL0
DSG0
DSL1
DSG1
360
TEST EXPECTED VALUE (FROM BIST CIRCUIT 30)
362
NR3
361
NR2
NR1
365
364
366
LATCH
368
TO TEST MEMORY 35
280
270
DOUT
304a
TST
320
ROW DECODER
322
BL
BL#
CL
WL
DBL0
DBL1
300
310
315
300d
305
RA
RE,WE
400S
SOURCE VOLTAGE GENERATING CIRCUIT
P0~P3
(BIST CIRCUIT / PROGRAM CIRCUIT)
410
Vcs
351
352
GND
350
340
DATA WRITE CIRCUIT
CA
304b
DIN
311
312

FIG.24

FIG.25

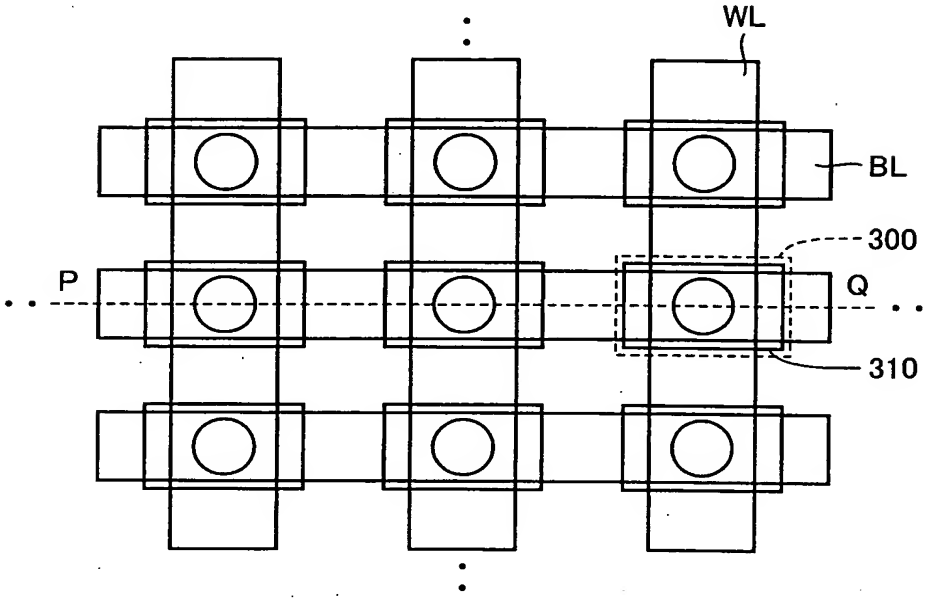


FIG.26

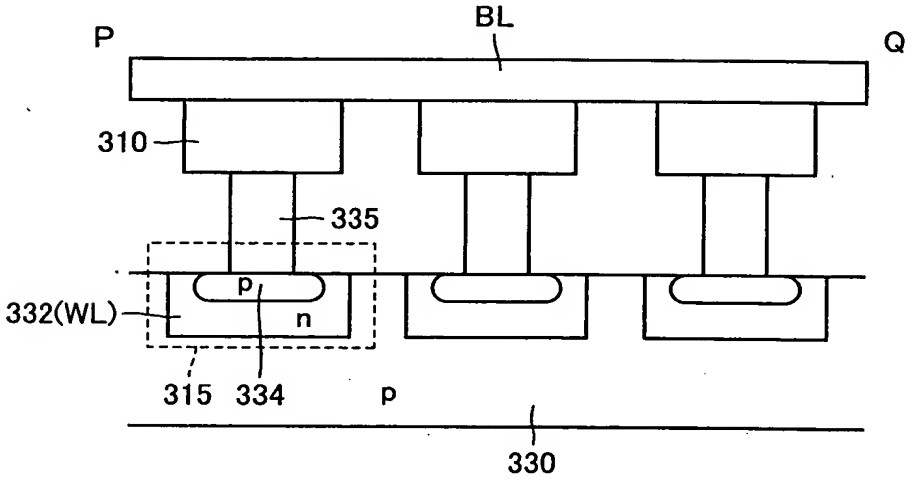


FIG.27

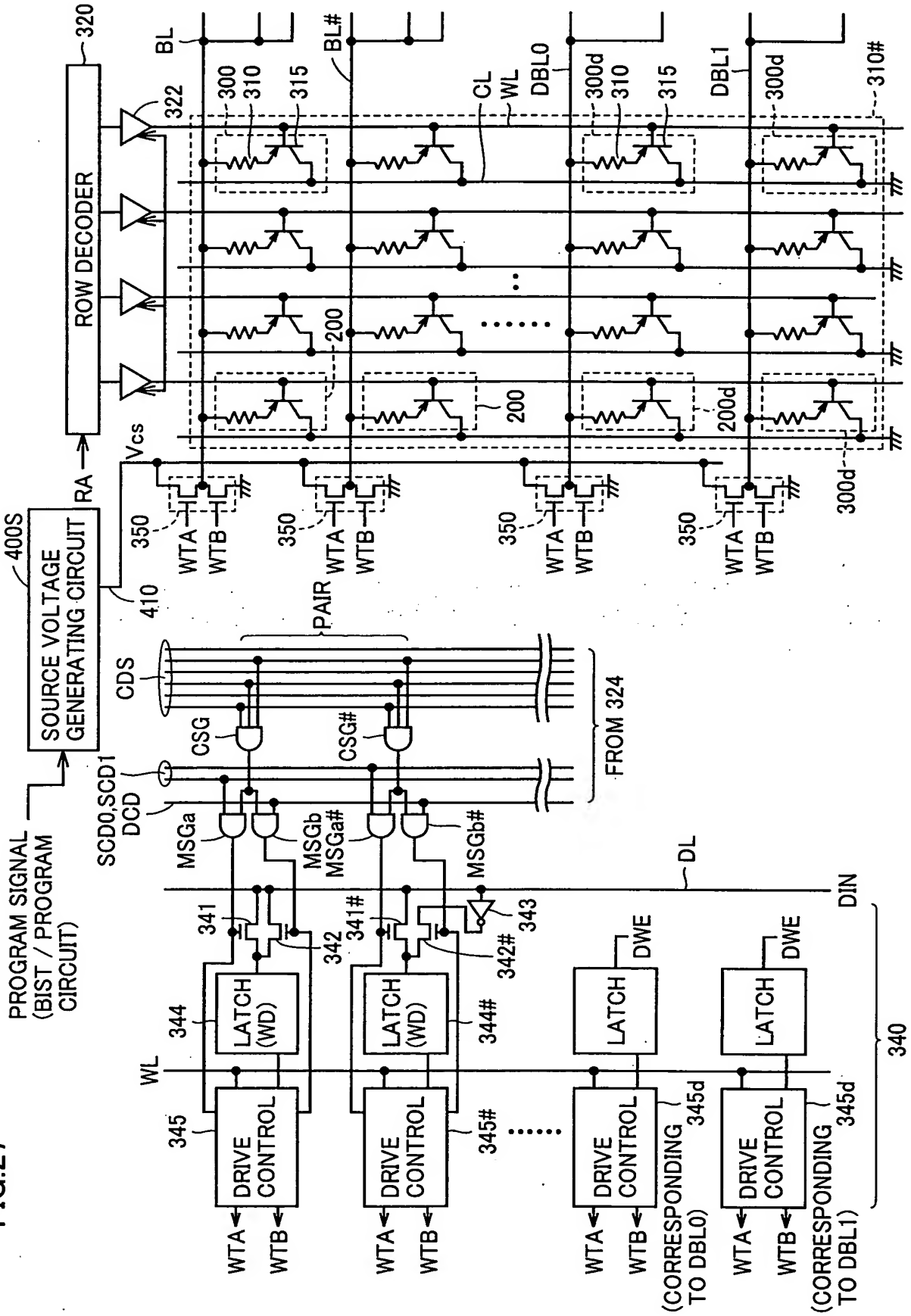

ROW DECODER
320
BL
BL#
DBL0
DBL1
CL
WL
300
310
315
322
200
200d
300d
310#
Vcs
RA
400S
SOURCE VOLTAGE GENERATING CIRCUIT
350
WTA
WTB
410
PAIR
CDS
CSG
CSG#
FROM 324
SCD0,SCD1
DCD
PROGRAM SIGNAL (BIST / PROGRAM CIRCUIT)
MSGa
MSGb
MSGa#
MSGb#
DL
DIN
341
341#
342
342#
343
344
344#
LATCH (WD)
LATCH
DWE
WL
345
345#
345d
DRIVE CONTROL
(CORRESPONDING TO DBL0)
(CORRESPONDING TO DBL1)
340

FIG.28B

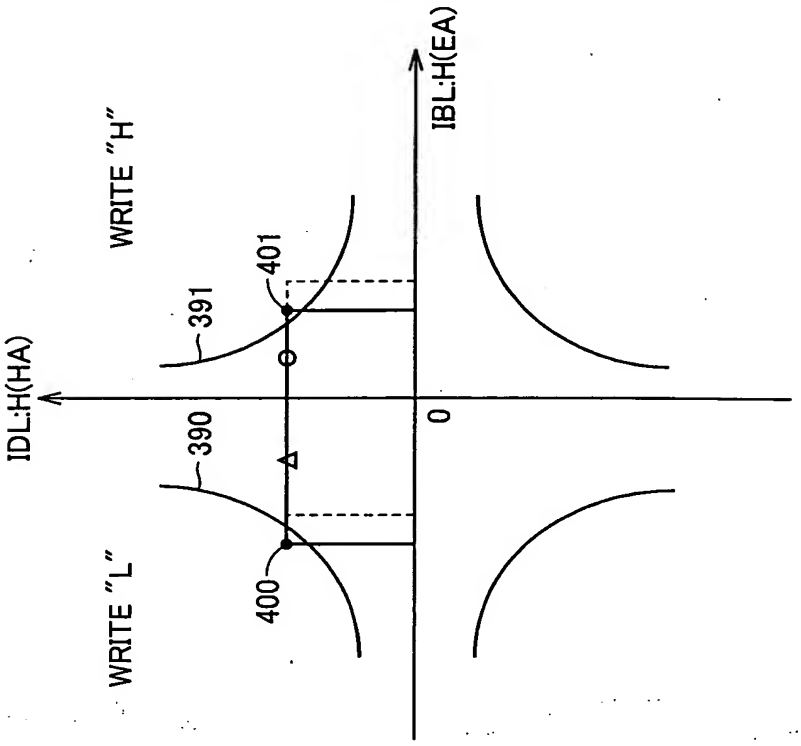


FIG.28A

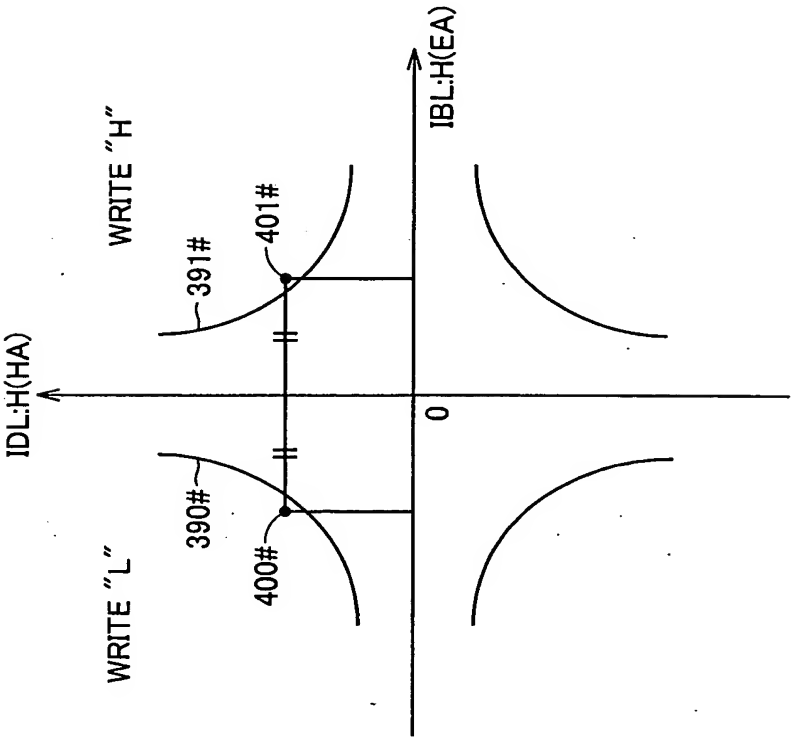


FIG.29A

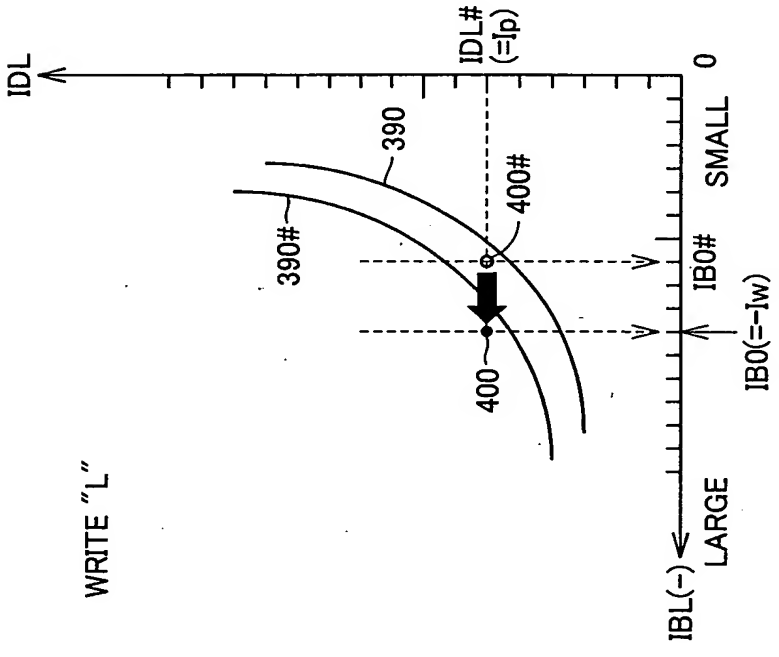


FIG.29B

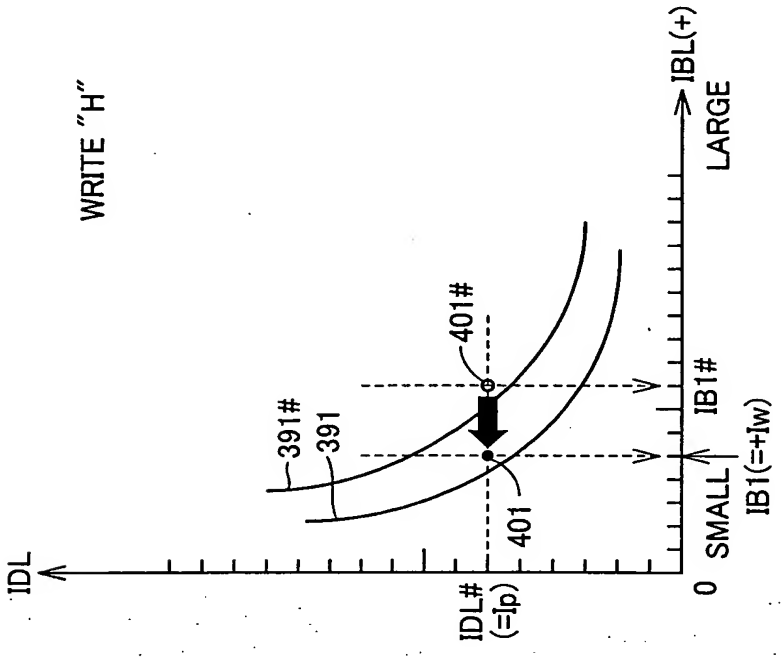


FIG.30

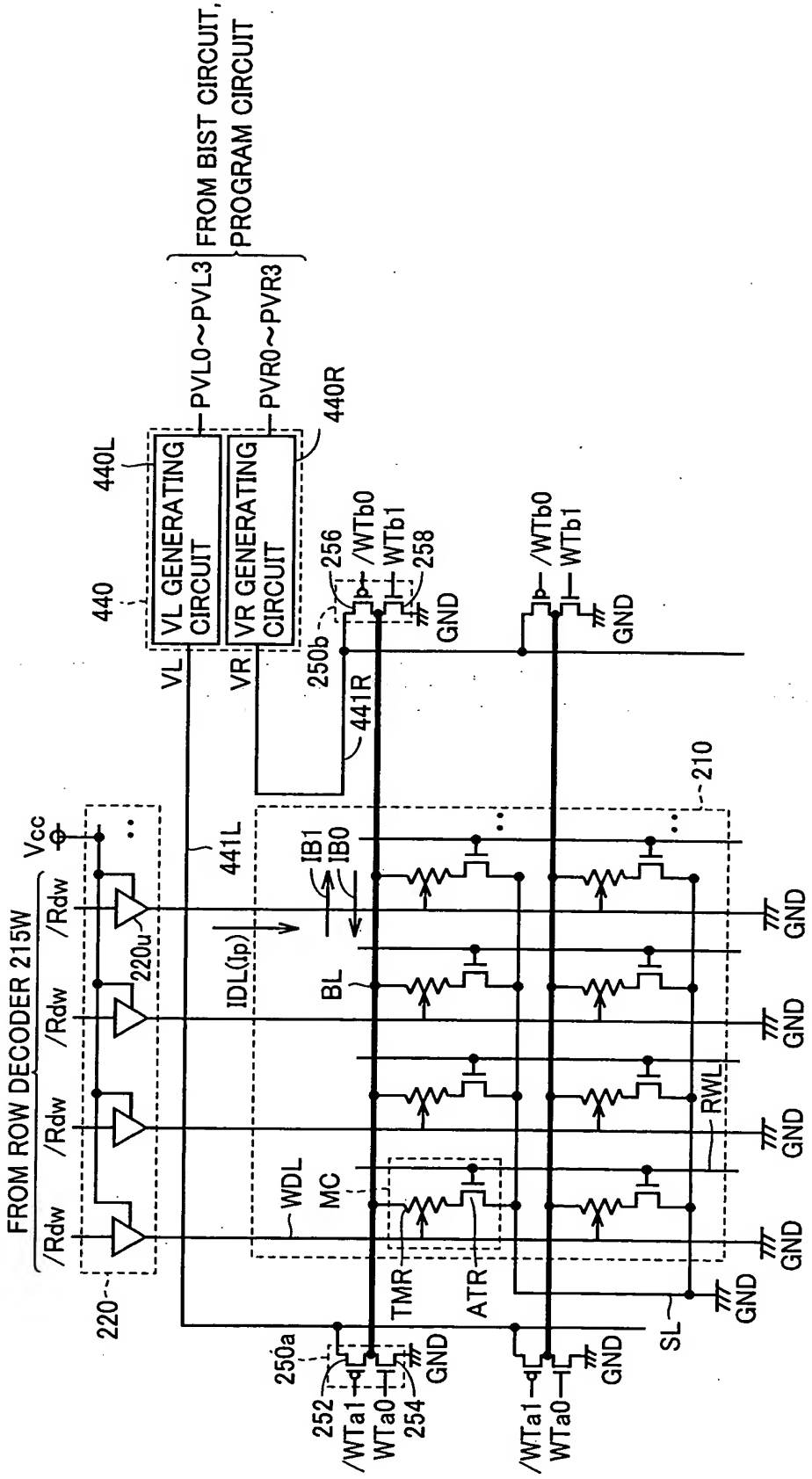

FROM BIST CIRCUIT, PROGRAM CIRCUIT
PVL0~PVL3
PVR0~PVR3
440L
440R
440
VL GENERATING CIRCUIT
VR GENERATING CIRCUIT
VL
VR
256
/WTb0
WTb1
258
GND
250b
441R
210
Vcc
441L
IB1
IB0
IDL(Ip)
BL
WDL
MC
RWL
TMR
ATR
SL
FROM ROW DECODER 215W
/Rdw
220u
220
250a
252
/WTa1
WTa0
254

FIG.31A

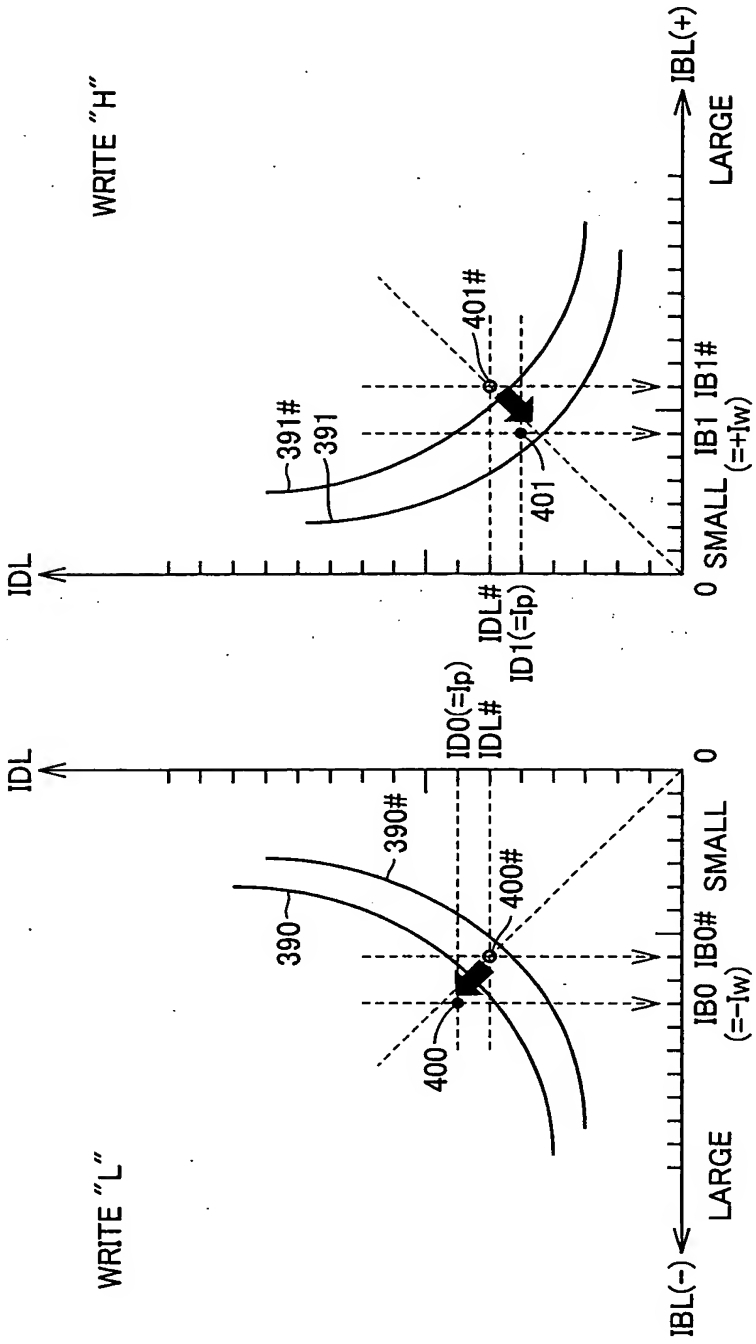


FIG.31B

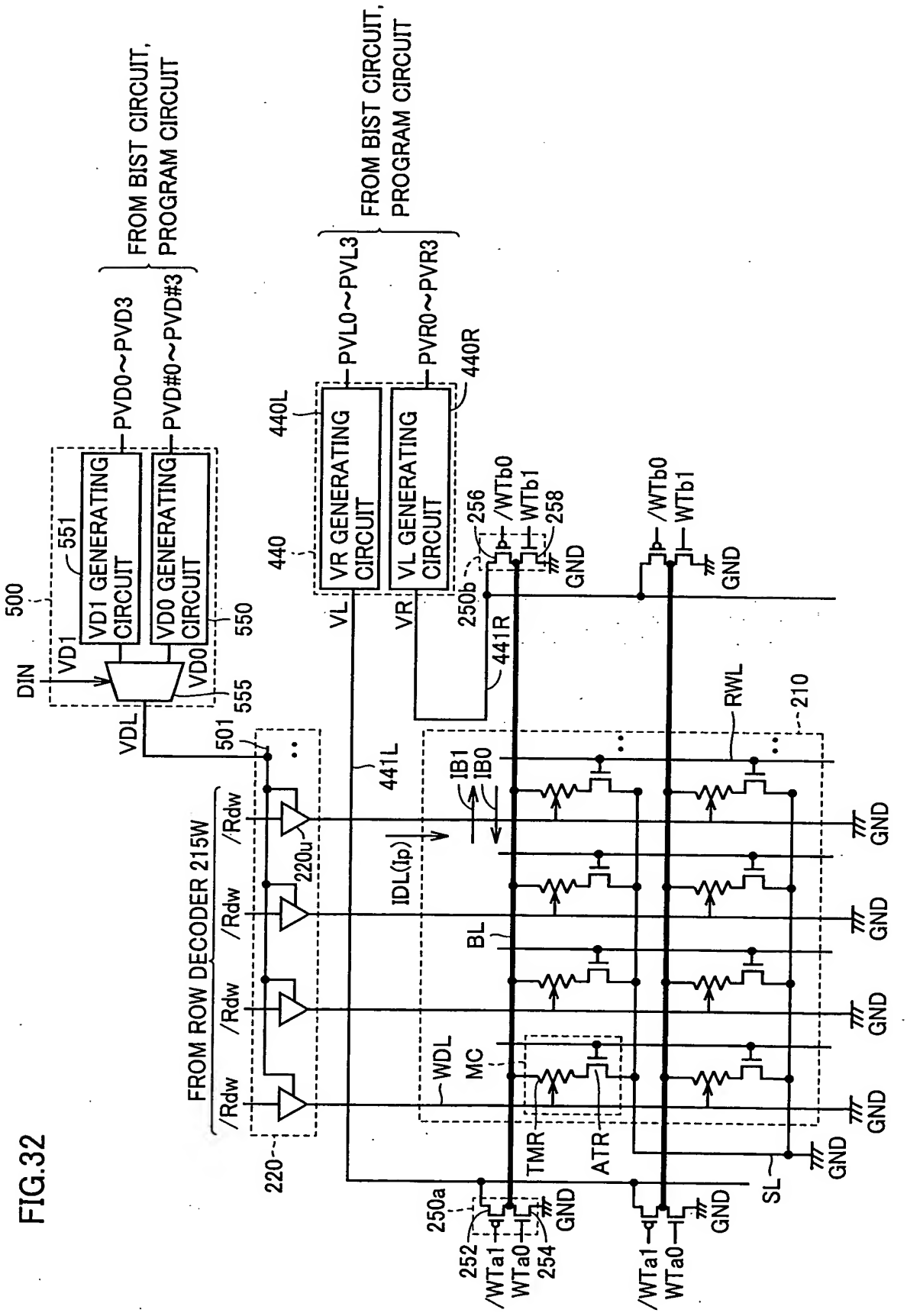

FROM BIST CIRCUIT, PROGRAM CIRCUIT
PVD0~PVD3
PVD#0~PVD#3
500
551
VD1 GENERATING CIRCUIT
VD0 GENERATING CIRCUIT
550
DIN
VD1
VD0
555
VDL
501
FROM ROW DECODER 215W
/Rdw
220u
220
440
440L
440R
VR GENERATING CIRCUIT
VL GENERATING CIRCUIT
PVL0~PVL3
PVR0~PVR3
VL
VR
441L
441R
250b
256
/WTb0
WTb1
258
GND
RWL
210
IB1
IB0
IDL(Ip)
BL
WDL
MC
TMR
ATR
SL
250a
252
/WTa1
WTa0
254

FIG.32

FIG.33

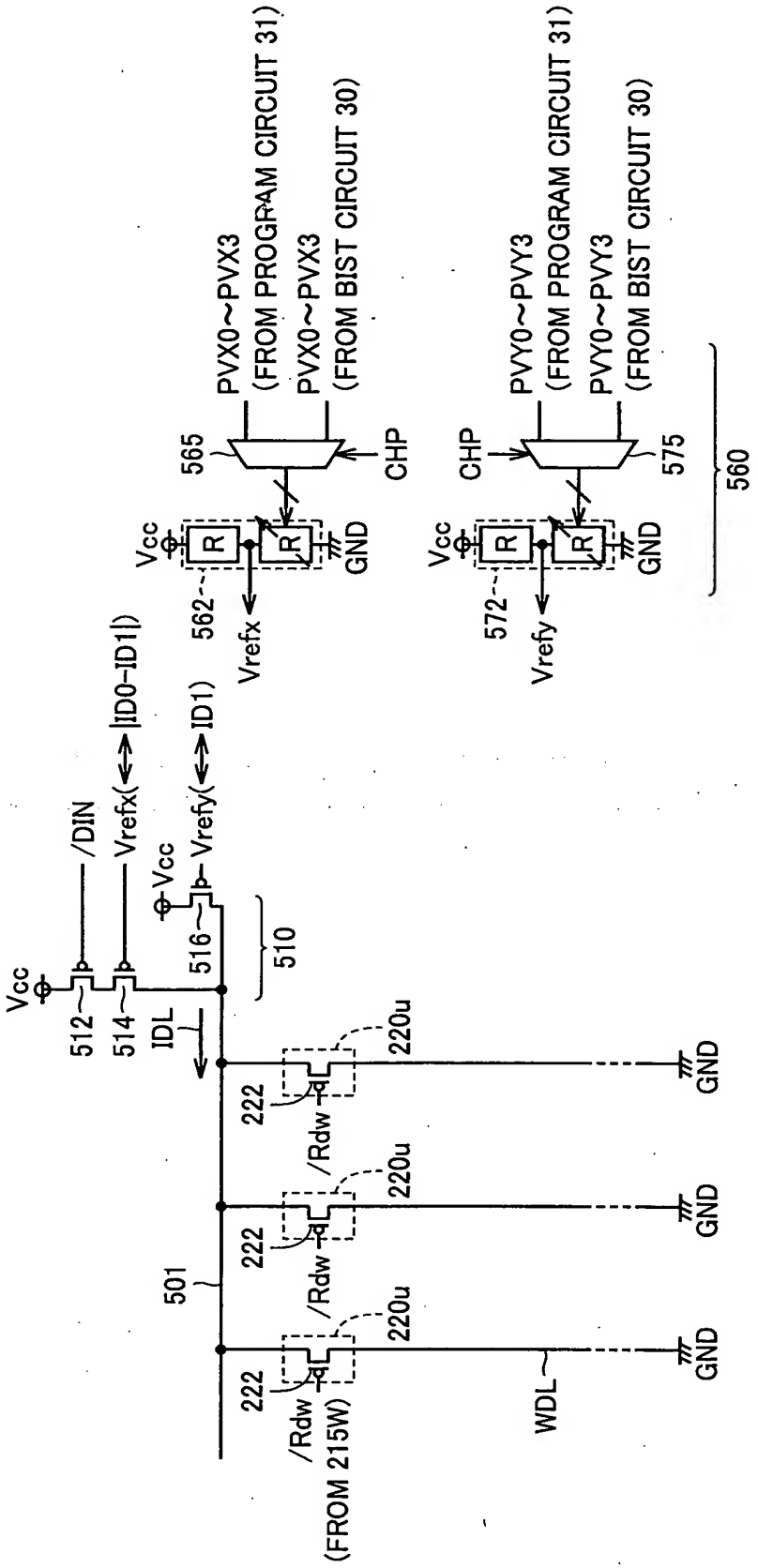

PVX0~PVX3 (FROM PROGRAM CIRCUIT 31)
PVX0~PVX3 (FROM BIST CIRCUIT 30)
565
CHP
Vcc
R
R
GND
562
Vrefx
PVY0~PVY3 (FROM PROGRAM CIRCUIT 31)
PVY0~PVY3 (FROM BIST CIRCUIT 30)
CHP
575
560
572
Vrefy
/DIN
Vrefx(↔|D0-ID1|)
Vrefy(↔ID1)
516
510
512
514
IDL
220u
222
/Rdw
501
(FROM 215W)
WDL

FIG.34

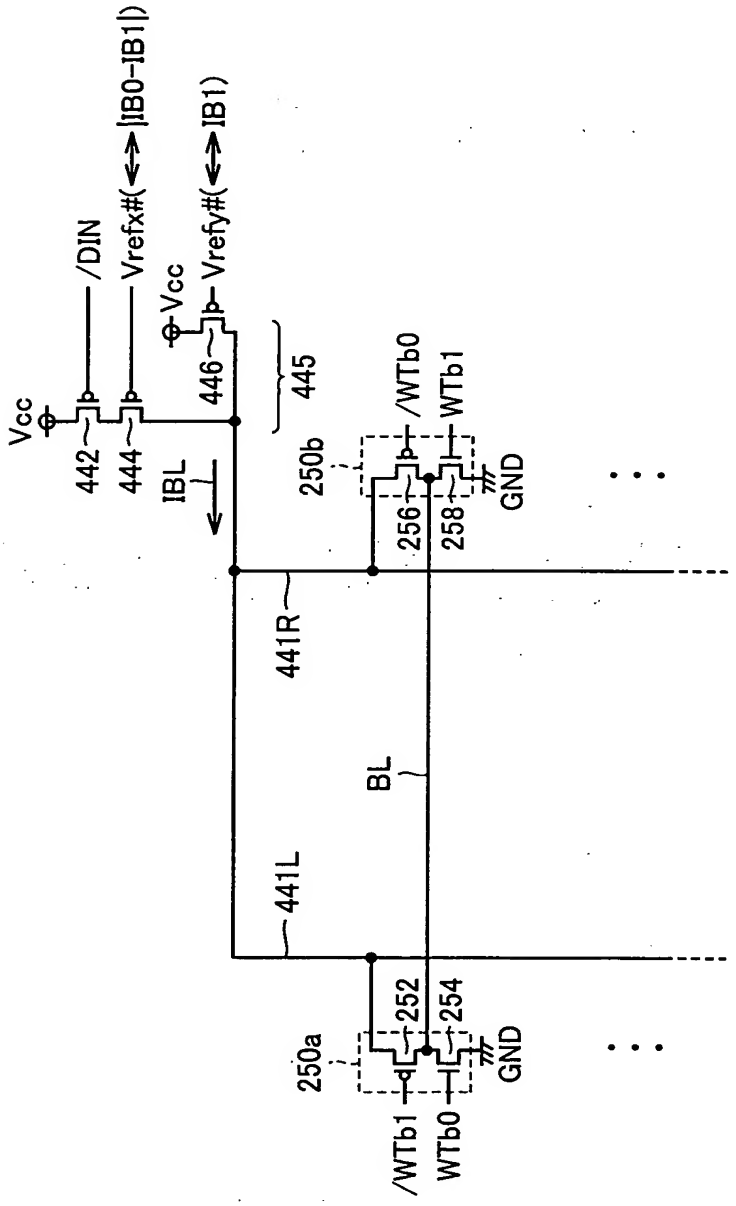

Vcc
/DIN
Vrefx#(↔|IB0-IB1|)
Vcc
Vrefy#(↔IB1)
442
444
446
445
IBL
250b
/WTb0
WTb1
256
258
GND
441R
BL
441L
250a
252
254
GND
/WTb1
WTb0

FIG.35

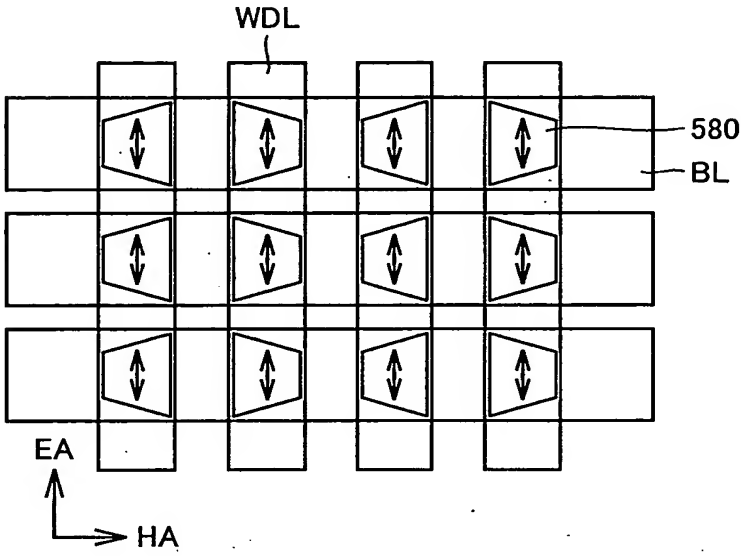


FIG.36

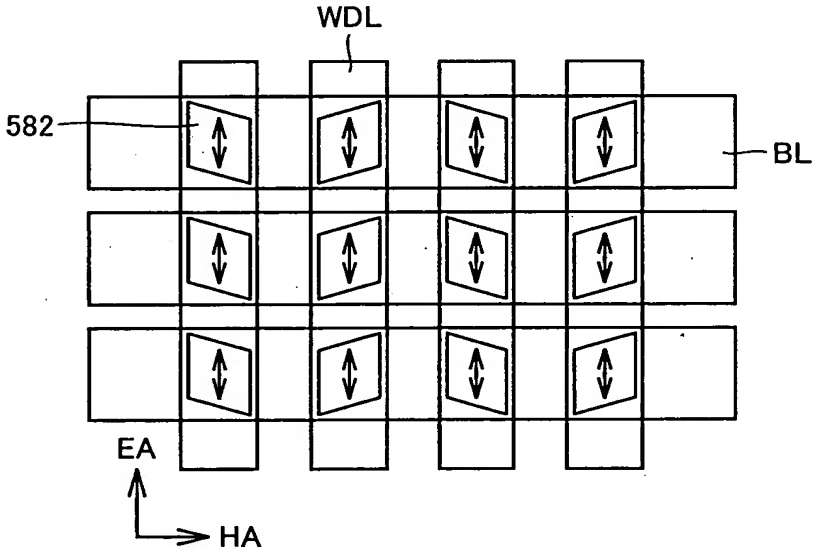


FIG.37

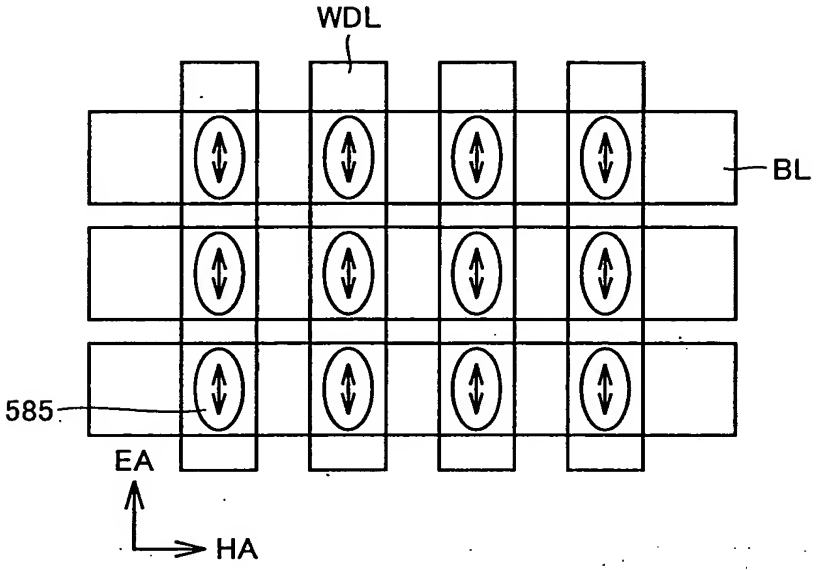


FIG.38A

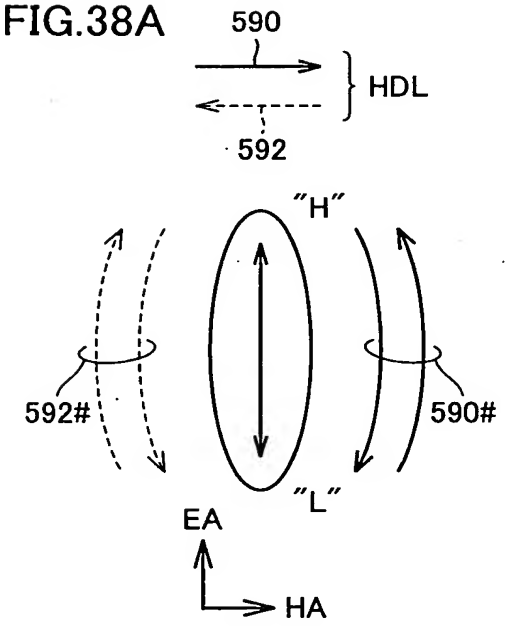


FIG.38B

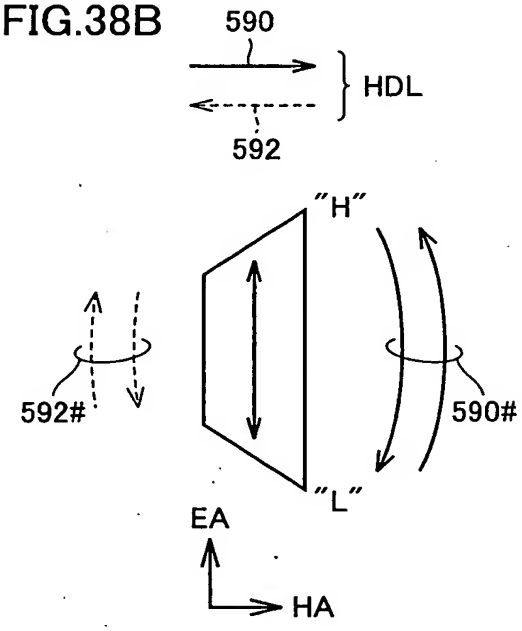


FIG.39A

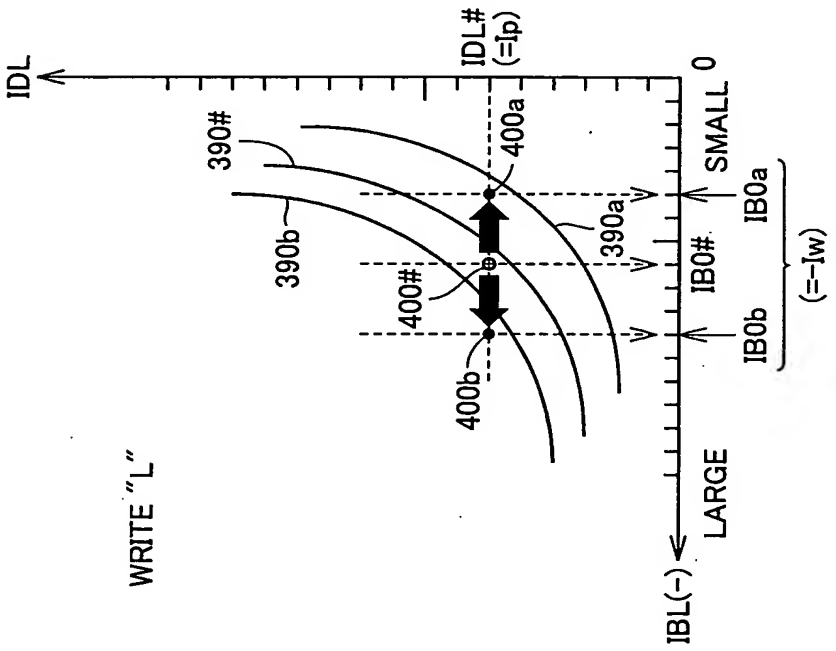


FIG.39B

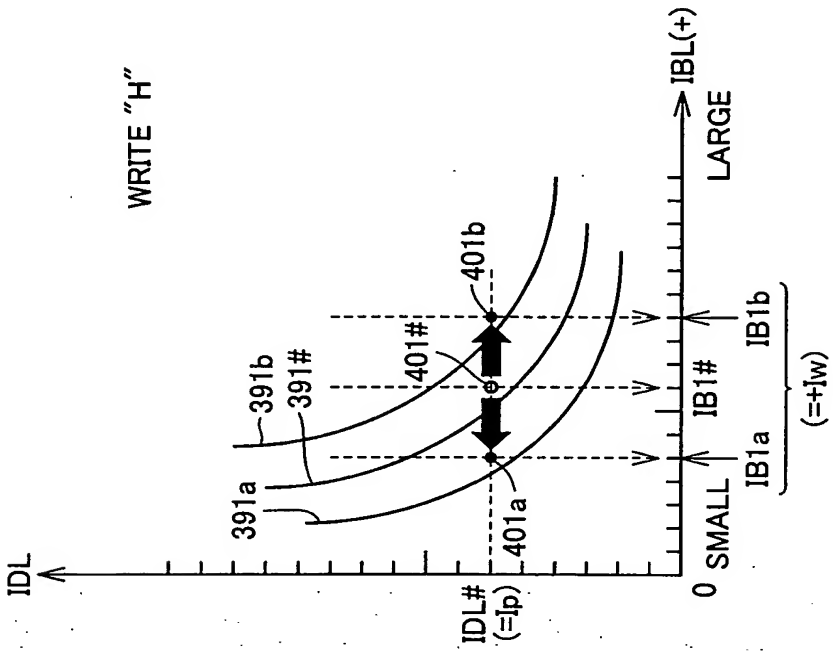


FIG.40

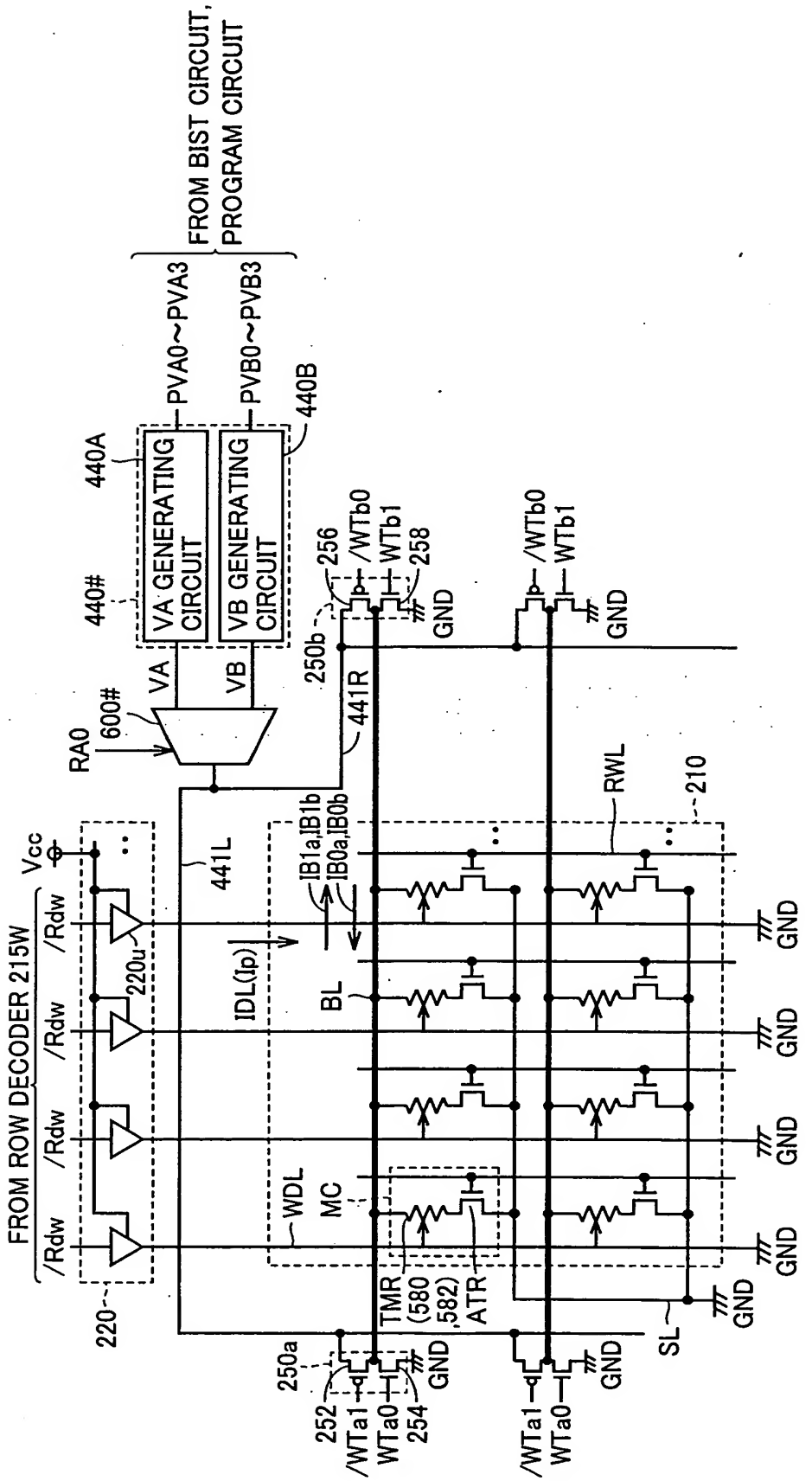

FROM BIST CIRCUIT, PROGRAM CIRCUIT
PVA0~PVA3
PVB0~PVB3
440A
440B
440#
VA GENERATING CIRCUIT
VB GENERATING CIRCUIT
VA
VB
600#
RA0
250b
256
/WTb0
WTb1
258
GND
441R
441L
RWL
210
Vcc
FROM ROW DECODER 215W
/Rdw
220u
220
IB1a,IB1b
IB0a,IB0b
IDL(Ip)
BL
WDL
MC
TMR
(580
582)
ATR
SL
250a
252
/WTa1
WTa0
254

FIG.41

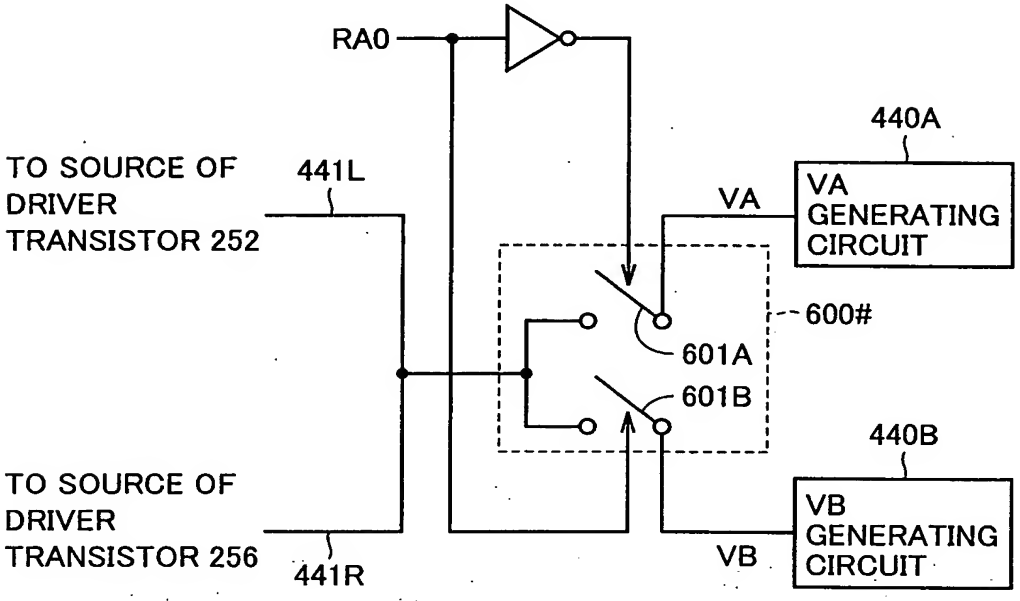

RA0
440A
TO SOURCE OF DRIVER TRANSISTOR 252
441L
VA
VA GENERATING CIRCUIT
600#
601A
601B
440B
TO SOURCE OF DRIVER TRANSISTOR 256
441R
VB
VB GENERATING CIRCUIT

FIG.42

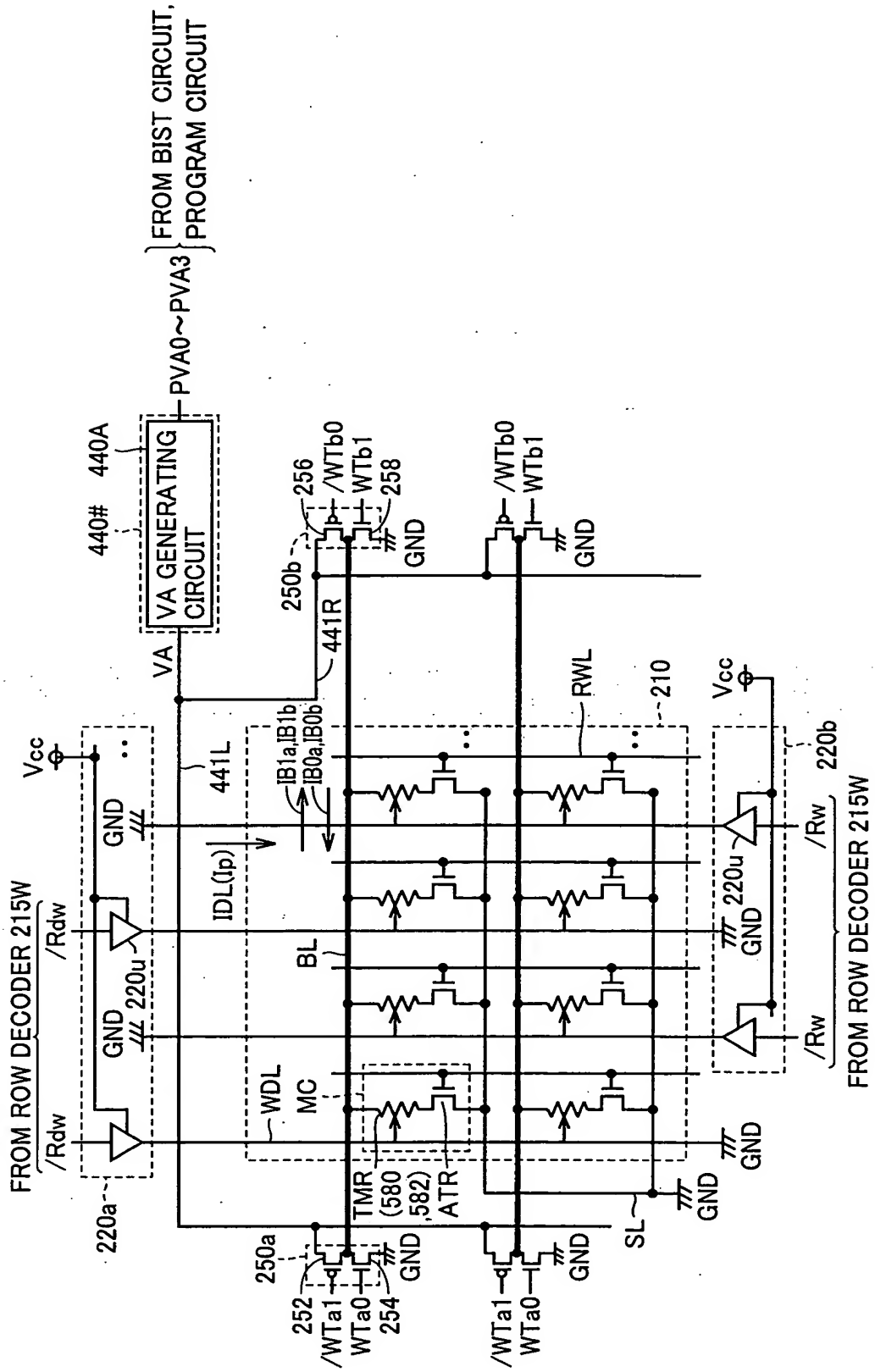

FROM BIST CIRCUIT, PROGRAM CIRCUIT
PVA0~PVA3
440A
440#
VA GENERATING CIRCUIT
VA
Vcc
GND
FROM ROW DECODER 215W
/Rdw
220u
220a
441L
441R
250b
250a
256
258
252
254
/WTb0
WTb1
/WTa1
WTa0
IB1a,IB1b
IB0a,IB0b
IDL(Ip)
BL
WDL
MC
TMR
(580
582)
ATR
SL
RWL
210
/Rw
220b
FROM ROW DECODER 215W

FIG.43A

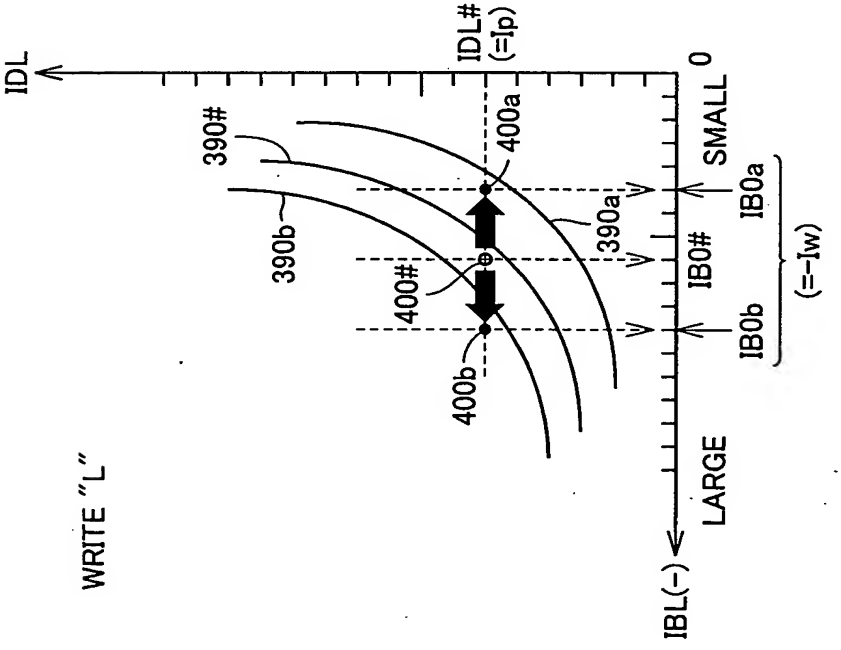


FIG.43B

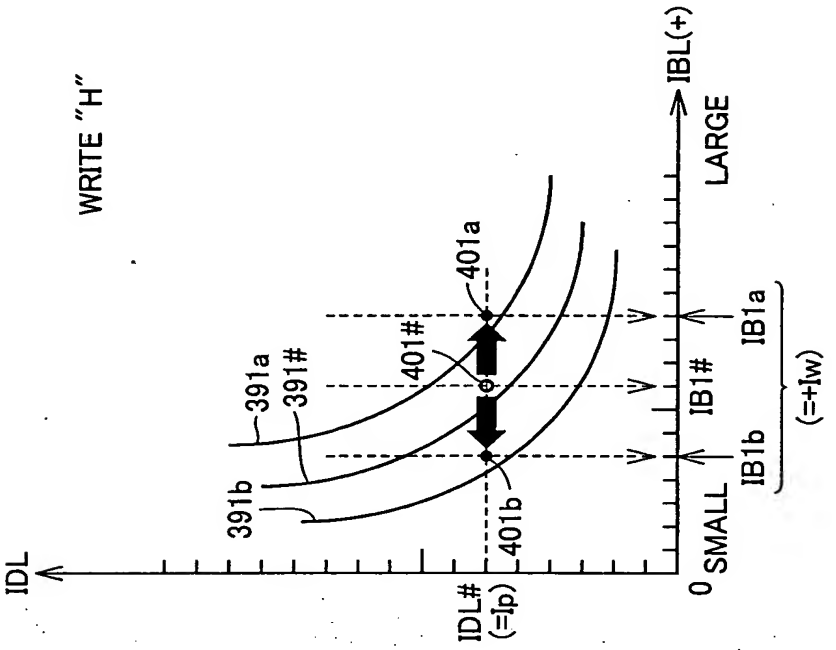


FIG.44

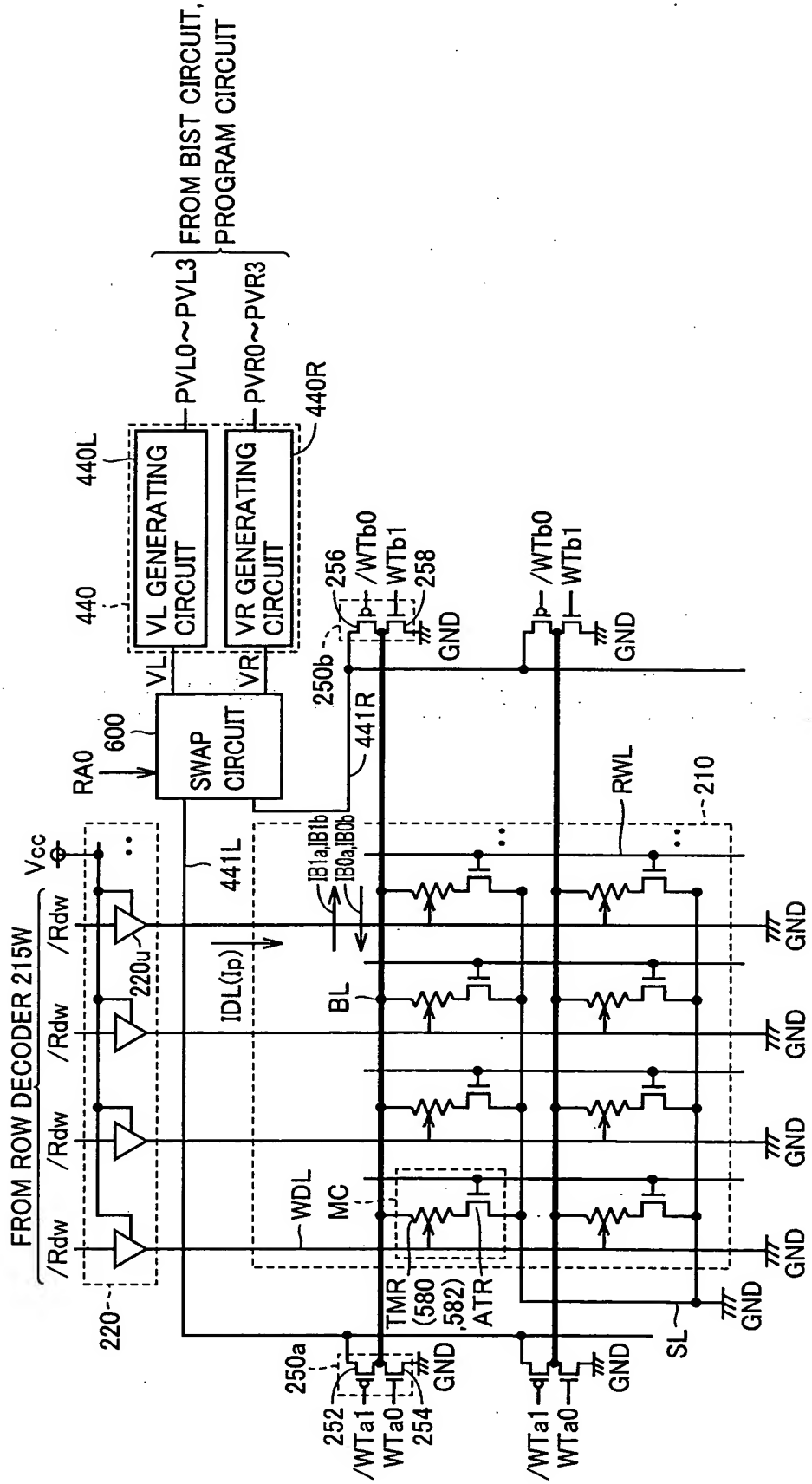

FROM BIST CIRCUIT, PROGRAM CIRCUIT
PVL0~PVL3
PVR0~PVR3
440L
440R
440
VL GENERATING CIRCUIT
VR GENERATING CIRCUIT
VL
VR
600
RA0
SWAP CIRCUIT
441L
441R
250a
250b
252
254
256
258
/WTa1
WTa0
/WTb0
WTb1
GND
Vcc
FROM ROW DECODER 215W
/Rdw
220u
220
IDL(ip)
IB1a,IB1b
IB0a,IB0b
BL
WDL
MC
TMR
(580 ,582)
ATR
RWL
210
SL

FIG.45

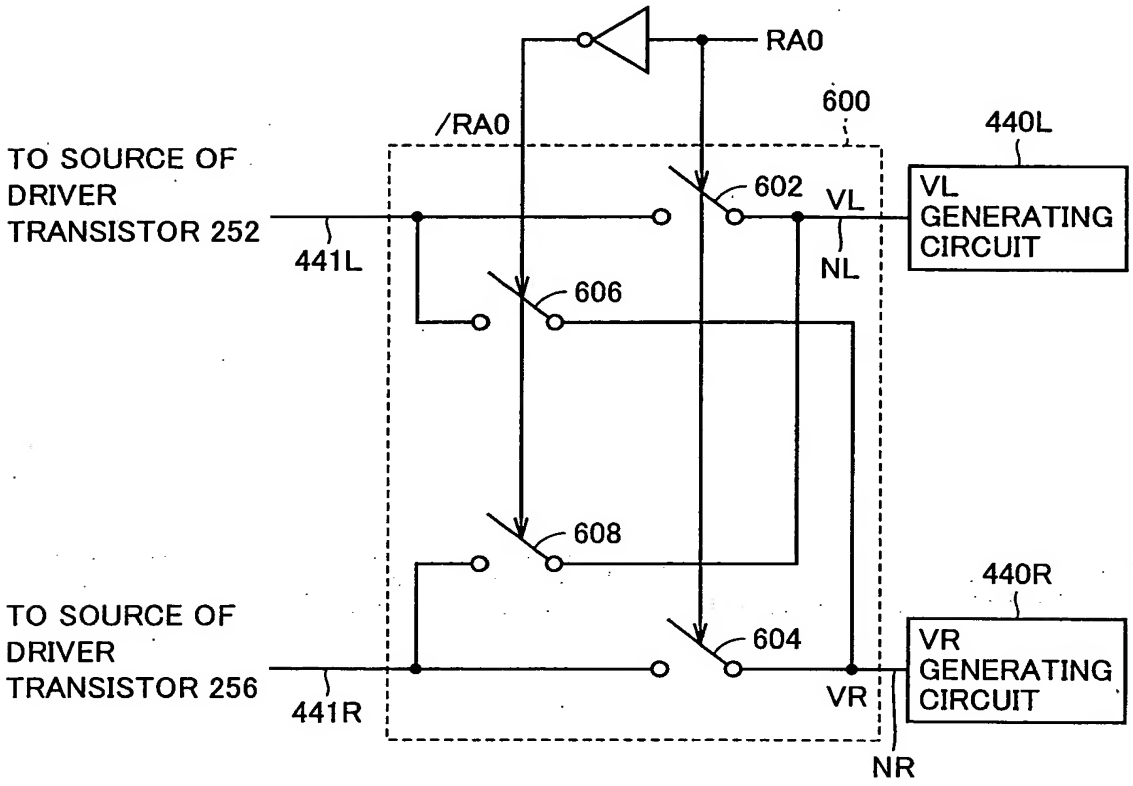

RA0
/RA0
600
440L
TO SOURCE OF DRIVER TRANSISTOR 252
441L
602
VL
VL GENERATING CIRCUIT
NL
606
608
440R
TO SOURCE OF DRIVER TRANSISTOR 256
604
441R
VR
VR GENERATING CIRCUIT
NR

FIG.46

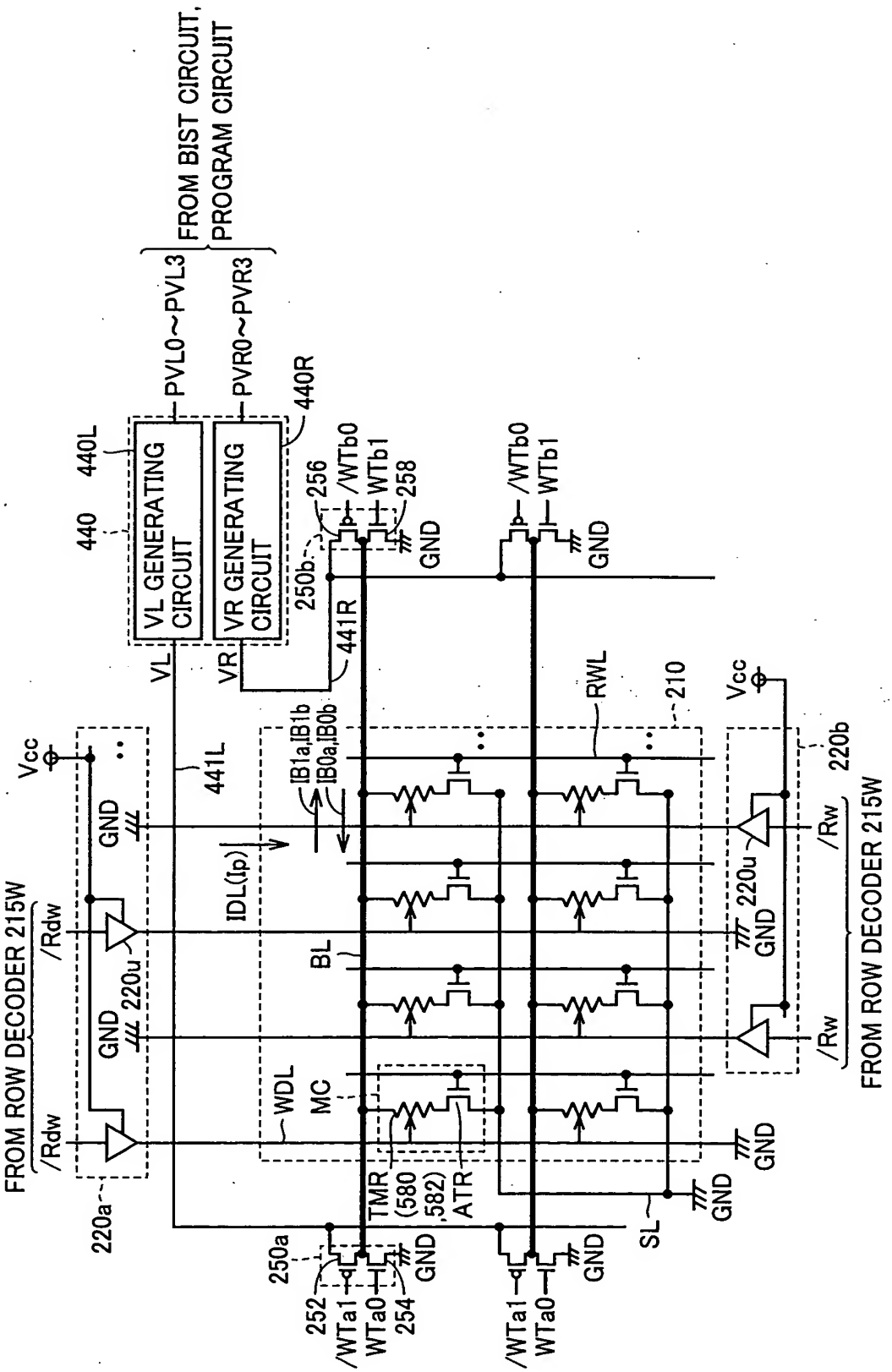
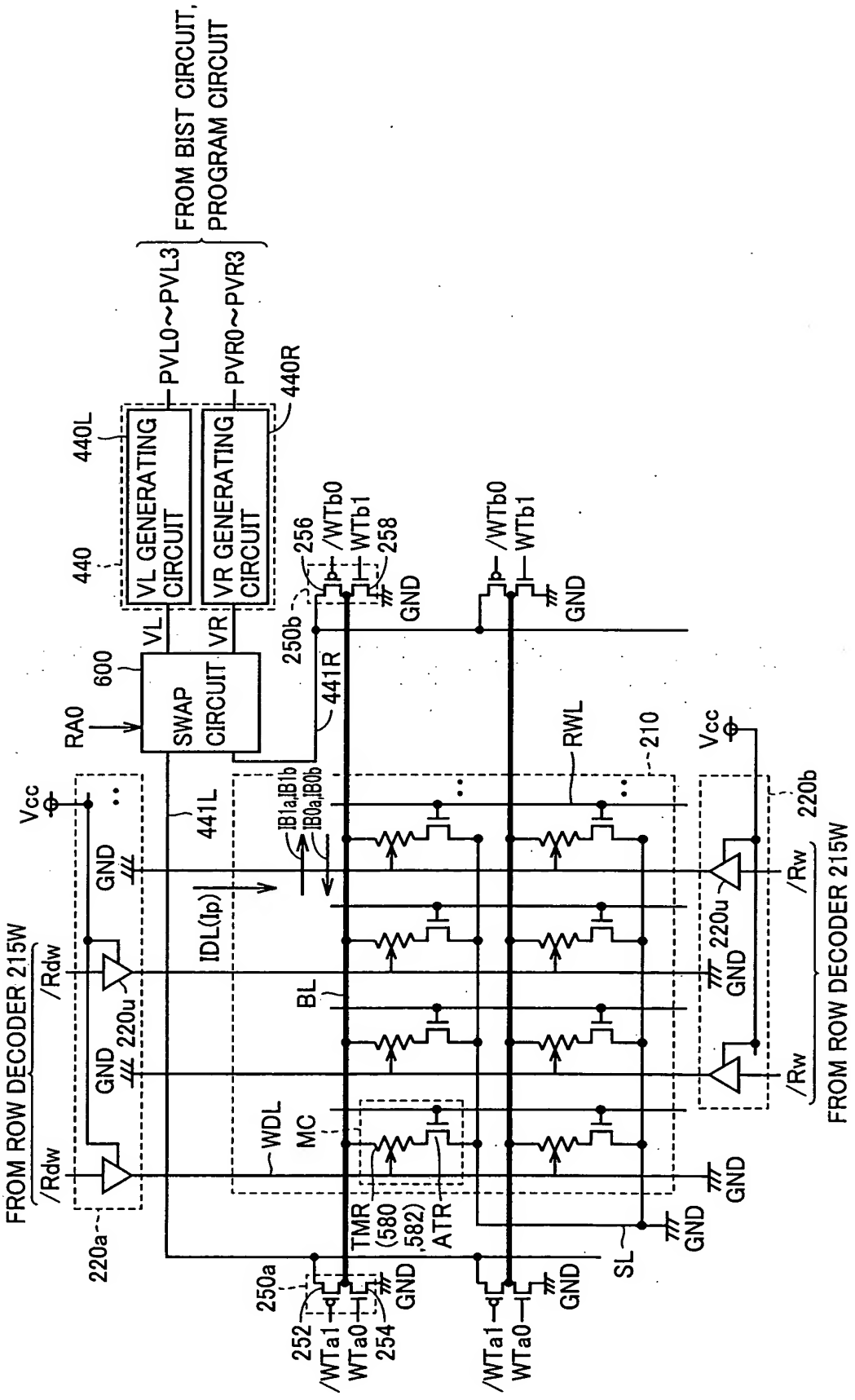

FROM BIST CIRCUIT, PROGRAM CIRCUIT
PVL0~PVL3
PVR0~PVR3
440
440L
440R
VL GENERATING CIRCUIT
VR GENERATING CIRCUIT
VL
VR
256
258
/WTb0
WTb1
GND
250b
441R
441L
IB1a,IB1b
IB0a,IB0b
IDL(Ip)
RWL
210
Vcc
220b
220u
/Rw
FROM ROW DECODER 215W
/Rdw
220a
BL
WDL
MC
TMR
(580
582)
ATR
SL
250a
252
254
/WTa1
WTa0

FIG.47


FROM BIST CIRCUIT, PROGRAM CIRCUIT
PVL0~PVL3
PVR0~PVR3
440L
440R
440
VL GENERATING CIRCUIT
VR GENERATING CIRCUIT
VL
VR
600
SWAP CIRCUIT
RA0
256
/WTb0
WTb1
258
GND
250b
441R
441L
RWL
210
Vcc
IB1a,IB1b
IB0a,IB0b
IDL(Ip)
BL
WDL
MC
TMR
(580
582)
ATR
SL
220a
220b
220u
/Rdw
/Rw
FROM ROW DECODER 215W
FROM ROW DECODER 215W
250a
252
/WTa1
WTa0
254